mmMoReEdge: A mmWave Modular and Reconfigurable Testbed Design using an Edge-Inspired Architecture

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ABSTRACT

We present mmMoReEdge, a modular and reconfigurable mmWave testbed inspired by edge computing architecture found in IoT devices. In mmMoReEdge, complex signal processing, typically required for 5G testing, is performed on the edge (local servers in close proximity) of a group of testbed nodes. mmMoReEdge offers modularity via configuration of phased-array antennas, RF front ends, ADC, and DAC, while the edge processing provides reconfigurability via scalable inline processing. We present simulation results that show that mmMoReEdge is 50% to 70% faster as compared to an offline CPU-based architecture and is 30% to 40% faster as compared to a node-based architecture with one FPGA.

KEYWORDS

Software Defined Networks, Software Defined Radio, 5G, IoT, Edge Computing, Modular, Reconfigurable

1 INTRODUCTION

The fifth generation (5G) cellular standard is being designed to support high-bandwidth and low-latency communication for a variety of IoT applications including health, transportation, manufacturing, and public safety. A key requirement to bring these use cases to fruition is the need for a modular and reconfigurable tested for testing these applications in configurations that closely mimic real-world situations. A testbed typically consists of three subsystems, namely: the acquisition subsystem, the computing subsystem, and the application subsystem. The acquisition subsystem contains components such as antennas, RF up- and down-converters, analog-to-digital converters (ADC) and digital-to-analog converters (DAC). The computing subsystem contains the processors and interconnect devices needed for processing the acquired signals. Finally, the application subsystem is the central hub for data management and user interaction. Software defined radio (SDR) based testbeds can be classified into these six categories, depending on how the processing subsystem is structured [1],

- General-purpose CPU (**GP**) approach: GP uses a central processing unit (CPU) based platform (PC) as the computing subsystem for offline processing. It provides flexibility and ease of use, but suffers from throughput constraints and non-real-time behavior due to the lack of determinism.
- Co-processor approach: This approach relies on the addition of a co-processor, such as a Graphical Processing Unit (GPU), to the GP approach to perform complex signal processing.
- Processor-centric approach: This approach uses dedicated processors for time-sensitive operations such as controlling TCP-IP layers. A conventional DSP, special purpose (custom-built) processors, and hardware accelerators are used to aid the central processor.
- Configurable units approach: In order to provide low energy consumption, this approach substitutes DSPs with special-purpose configurable units.
- Programmable blocks (**PB**) approach: PB uses programmable blocks, mainly FPGAs with or without embedded processors. It provides great flexibility to create tailored architectures via reconfigurability. Programmable blocks offer high computing power for moderate energy consumption.
- Distributed approach: Custom testbeds based on a distributed computing approach, where the complex signal processing is spread out to a farm of processing elements on the Internet.

The concept of edge computing is a key part of the 4-stage Internet of Things (IoT) solutions architecture [2]. Edge computing has been gaining prominence lately as it enables data-stream acceleration, including real-time data processing without latency. It allows smart applications and devices to respond to data almost instantaneously as its being acquired. It allows for efficient data processing as large amounts of data can be processed near the source, reducing Internet bandwidth usage. This approach eliminates costs and ensures that applications can be used effectively in remote locations. Additionally, the ability to process data without ever putting it on a public server adds a useful layer of security for sensitive data.

In this paper, we use the principles of edge computing to propose a new testbed system design ideally suited for testing 5G enabled IoT applications. This testbed, called mmMoReEdge, offers real-time reconfigurability with online processing to enable mmWave 5G tests. Reconfigurability at the software layer allows the system to adapt to different gain profiles, channel conditions, and antenna configurations. Modularity at the hardware level enables the acquisition and computing subsystems to leverage new commercially-available, off-the-shelf components as they become available, enabling the system to be scalable to meet evolving requirements. We compare the performance of mmMoReEdge with GP and PB approaches for different use cases representing low, medium, and high complexity signal processing and present simulation results for the same. The key contributions of this paper are:

- We present the system-level design of mmMoReEdge, a modular and reconfigurable testbed inspired by the edge computing architecture. We describe the key components of the testbed node, testbed edge, and the host PC and discuss the how these components are interconnected.
- We present a mathematical model for the parameter *processing time*, which is used as the key metric to compare mmMoReEdge with the GP and PB architectures.
- We describe three different use cases. Namely, we include measurements for IQ Power, Complex FFT Spectrum, and Angle of Arrival as a representation for low, medium, and high complexity signal processing. Processing time for these three measurements is used as the metric for comparison.
- We present simulation results which demonstrate that mmMoReEdge outperforms the GP and PB approaches for medium- and high-complexity use cases. For example, mmMoReEdge is 50% to 70% faster as compared to the GP approach and is 30% to 40% faster as compared to the PB approach.
- We provide source code as an artifact associated with the paper. This source code will allow researchers to reproduce the simulations to validate our results and expand it for future work.

2 5G TESTBED PERFORMANCE METRICS

The design of any testbed can be optimized around the vectors of throughput, hardware agility, scalability, cost, and latency [3]. Throughput of the test system can be described as the ability to transmit and/or receive data at a desired rate. It is mainly driven by the real-time bandwidth of the radio front end, ADC sampling rate, heterogeneous processing, and bus architecture. Hardware agility can be described as the ability of the system to reconfigure its input at runtime, using parameters such as frequency, power level, and sampling rates. Hardware agility is also useful for reconfiguring digital input lines controlling the antenna subsystem. Scalability can be described as the ability of the testbed to extend its use for future applications without major re-design. Cost is usually measured as the total cost of ownership, which is a function of the purchase, development, and maintenance costs. Finally, latency is characterized by both the speed and deterministic nature of processing. It is influenced mainly by two factors: the type of computing nodes used and the bus technology between the computing nodes.

While the metric of latency can be interpreted in multiple ways, we are most interested in the amount of time it takes for the test system to make a decision based on acquired data, referred to as processing time. For the purpose of comparing different testbed architectures, in this paper we model the processing time metric using Equation 1:

$$T = (t_a) + \sum_{i=1}^{N}((S_i/B_i) + (M_i/(P_i * k_i)) + \delta_i) \quad (1)$$

Here, we use the following notations:

- t_a is the acquisition time in seconds.
- S_i is the number of samples being transmitted between the source and sink node for a particular computing platform.
- B_i is the bandwidth in Samples/Second for the bus technology to transmit these samples, $B > 0$.
- M_i is the number of operations needed to make the decision.
- P_i is the processing power of the computing platform in operations/second, $P > 0$.
- k is a scaling factor based on the amount of available processing capability, $0.1 \leq k \leq 1.0$.
- δ_i is an additional delay introduced depending on the non-deterministic behavior of the computing platform. In this paper, we will only use a qualitative value for this parameter to highlight the level of determinism in the processing time.
- N is the number of processors in the testbed.

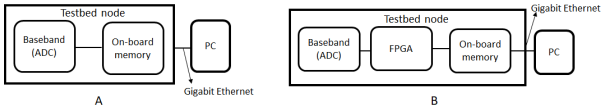

Figure 1: Fig. A: GP Architecture, Fig. B: PB Architecture

The architectures for testbeds using the GP approach and the PB approach are shown in Figure 1. In this paper, we will compare the performance of the proposed mmMoReEdge testbed with these two architectures, as they closely mimic the cloud computing and node-only computing architectures found in IoT systems.

In the GP architecture, there is no processor on the testbed node. The only processor is on the PC. Hence, N is set to 1. The source node is the on-board memory on the node, and the sink node is the memory on the PC. We assume a Gigabit Ethernet bus between the source and the sink. For the purpose of this comparison, we use a laptop with an Intel(R) Core(TM) i7-6820HQ, where the quad-core CPU is running at 2.70 GHz with 8 logical processors as the PC. Even though this is a multi-core CPU, we assume that the measurements will be run with highest priority on one core, thereby reducing the variability in the processing time. With these assumptions, we set $N = 1$ and the values for different parameters in Equation 1 are shown in Table 1.

Table 1: Values of Parameters for General Purpose CPU Approach

Parameter	PC
k	1.0
B	1e9
P	2.7e9
δ	Medium-High

In the PB architecture, traditionally, there is one FPGA on the testbed node, such as the one implemented using an FPGA-based USRP from Ettus Research, in addition to the processor on the PC. Hence, N is set to 2. The source node for the first processor is the ADC on the node, and the sink node is the FPGA. The bus technology connecting these two is typically a high-speed serial protocol such as Serial RapidIO or Aurora. The signaling rate for sRIO is 1.25, 2.5, or 3.125 Gbps per a differential transmit and receive pair. A protocol like Aurora can offer higher speeds but comes at higher

complexity. For FPGAs, we consider a configurable microprocessor/microcontroller architecture supported on most FPGA families, including the Zync7000 from Xilinx [4]. This supports a processing speed of 240 DMIPS (Dhrystone million instructions per second). However, anywhere between 50% to 90% percent of this FPGA may be utilized by the instrument provider for control and configuration, thereby leaving only a small fraction of the resources for processing [5]. The source node for the second processor is the on-board memory on the node, and the sink node is the memory on the PC. For our comparison, we will assume that the node only has one on-board FPGA. With these assumptions, we set $N = 2$, and the values for different parameters in Equation 1 are shown in Table 2.

Table 2: Values of Parameters for Programmable Blocks Approach

Parameter	Node	PC
k	0.1-0.5	1.0
B	2.5e9	1e9
P	270 DMIPS	2.7e9
δ	Low	Medium-High

Next, we describe the three measurements, along with their use cases, that we have considered for evaluating the processing time metric. We have considered these three measurements as they represent low-, medium-, and high-complexity computations, respectively.

- IQ Power Measurements (Low-Complexity): As 5G will require radiated signal tests, it is important to measure the Peak-to-Average Power Ratio (PAPR) of the received signal and operate the receiver within its linear operating range. A 5G testbed should have the ability to measure the PAPR of the incoming signal and adjust the maximum operating power of the testbed to maximize the dynamic range. This is typically done using the IQ power measurement calculations.
- Complex FFT Spectrum (Medium-Complexity): This measurement calculates the magnitude and phase (relative to a reference) of the signals as a function of frequency. For 5G applications, measurements have to be done within the coherence time, wherein the channel state can be considered to be constant. Due to this, a 5G testbed should have the ability to make fast and repeatable measurements within a fixed time period.
- Angle of Arrival using MUSIC algorithm (High-Complexity): Directionality will be a key feature of 5G networks for beam forming and beam steering capabilities. To closely mimic real-world scenarios, a 5G testbed should be able to make angle of arrival measurements and use this information as control signals to adjust the RF front end for different beam parameters.

3 PROPOSED TESTBED SYSTEM DESIGN

In this section, we describe the system design of the proposed testbed, called mmMoReEdge, which consists of a bank of testbed nodes, the testbed edge, and the host PC, possibly connected to the cloud as shown in Figure 2. This design has been inspired by edge computing, which is a distributed and open information technology (IT) architecture that features decentralized processing power. In this architecture, data is processed on a local processor in close promixity (called edge) of the node. Figure 2 shows the system-level design of mmMoReEdge.

A group of testbed nodes can be used to form a bank, wherein each node contains antennas that are attached to a mmWave subsystem (subsystem A) that allows for frequency translation to and from mmWave frequenices to the sub-6 GHz frequency range. The testbed has been designed to adapt to multiple frequency bands from 28 to 76 GHz. The baseband (ADC, DAC) subsystem (subsystem B) operates at sub-6 GHz frequencies and manages the analog-to-digital and digital-to-analog conversion at wider bandwidths. The on-node FPGA (subsystem C) provides hardware configuration and manages the directivity controls on the antennas, based on a feedback loop. It also provides co-processing for inline signal processing and analysis to be performed on the node, based on the number of available resources.

To enable additional inline signal processing and fast measurements, mmMoReEdge provides the concept of a testbed edge, similar to the concept of edge devices. The testbed edge aggregates data from a number of nodes and delivers additional inline processing power as shown in Figure 2. The testbed edge can have multiple FPGAs all interconnected via high-speed serial transceivers. The communication mechanism between the nodes and the edge is shown as cabled PCIe but also can be adapted to high-speed serial I/O for high data rate applications. Networking is provided through Linux RT based node computers, which then communicate with the host PC for application-layer support. The host PC also provides connectivity to the cloud for data storage and post processing. With the assumption of one testbed node, one FPGA per testbed edge, and one PC, we set the value of N to 3, and the values for different parameters in Equation 1 are shown in Table 3.

Table 3: Values of parameters for one configuration of proposed design

Parameter	Node	Edge	PC
k	0.1-0.5	0.9	1.0
B	2.5e9	2e9	1e9
P	270 DMIPS	270 DMIPS	2.7e9
δ	Low	Low	Medium-High

A practical implementation of the testbed edge can be demonstrated using the NI ATCA-3671, which features four user-programmable Virtex-7 690T FPGAs. It has four slots for both analog and high-speed serial I/O options. Inter-FPGA communication is achieved via high-speed serial transceivers, maintaining a maximum data rate of 12.5 Gb/s. It supports 16 lanes to adjacent FPGAs and 12 lanes to diagonal FPGAs. The ATCA-3671 is programmable with the LabVIEW FPGA Module and BEEcube Platform Studio [6].

Reconfigurability of the hardware elements is a key feature of the testbed and enabled by the control and processing software running on the FPGAs. The testbed is programmable across all the

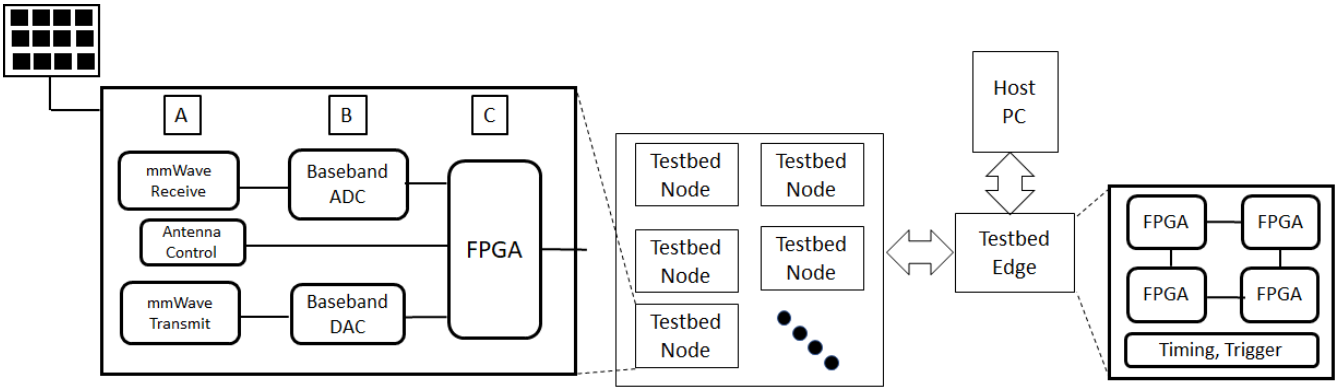

Figure 2: mmMoReEdge, a mmWave MOdular and REconfigurable testbed inspired by Edge computing architecture.

PHY-MAC TCP-IP layers and the instrumentation layers via a well-defined Application Programming Interface (API). For example, the physical layer API is responsible for controlling the modulation scheme, symbol rate, filter type, channel response equalization filter taps, or coding parameters. It also monitors the received signal characteristics, such as RSSI, and provides feedback to the upper layers. The testbed has been designed such that it allows for real-time configuration of the radio layer parameters. The Measurement Abstraction Layer API is responsible for configuring the testbed for different measurements and parameters specific to the controlling instrument, such as frequency, power level, and instantaneous bandwidth (specified as sampling rate).

Flexibility at the baseband level is enabled via the use of Software Defined Radios (SDRs) such as USRP [7]. NI-USRP 2944 supports 160 MHz instantaneous bandwidth with a carrier frequency range of 10 MHz to 6 GHz, referred to as sub-6 GHz in the remainder of this paper. The sub-6 GHz band serves as the baseband system of our testbed and provides frequency coverage and reconfigurability for research on topics such as the LTE-to-5G migration, LTE-5G co-existence, and IoT applications. The modular nature of our testbed node's mmWave heads addresses the challenges related to different frequency bands being considered [8, 9] for various 5G applications. For example, 5G New Radio (5G NR) is taking shape in 3GPP with OFDM-based Unified Flexible Radio Access Technology below 40 GHz [10]. Likewise, a 5G/KT mmWave specification with a preliminary 5G standard is also being released for for 28 GHz fixed-wireless access. Our testbed allows the sub-6 GHz sub-system to be extended with mmWave up- and down-converters for different frequency bands.

Many of the new 5G implementations will require beam steering on multiple beams. Hence, as advanced beam steering technology is developed and integrated into new 5G designs, mmMoReEdge can be easily adapted using the Antenna Control subsystem in Figure 2. It has been designed to support beam forming and beam steering on multiple beams. The design contains digital lines from the FPGA to the antenna control sub-system, which can control both the phased-array antennas and mmWave transmit/receive sub-systems. The reconfigurable aspect of the testbed allows the user to select digital codes specific to the desired phase value using FPGAs on the node and then control subsystem A. Some of the options considered for phased-array antennas include Anokiwave [11], Sage [12], SensorView [13], and Taoglas [14].

4 EVALUATION RESULTS

In this section, we present simulation results that use the processing time required for the three measurements described in Section 2 to compare the performance of GP, PB, and mmMoReEdge testbeds. The processing time is calculated as per Equation 1 with values of different parameters as defined in Tables 1, 2, and 3.

4.1 Processing Time for Different Measurements

The number of real-valued multiplications and additions required to perform a particular measurement is used to determine the value of M in Equation 1. While additional operations may be involved, we assume that the real-valued multiplications and additions serve as a practical proxy for our comparison purposes. The IQ Power measurement, used for adjusting the gain and reference values on the RF front end, have modeled this using Equation 2.

$$P^2 = I^2 + Q^2 \tag{2}$$

As seen, it has two real-valued multiplications and one real-valued addition for each measurement sample. Hence, the value of M for this measurement is set to 3 per measurement sample. The second measurement being used for comparison purposes is the Complex FFT Spectrum for magnitude and phase calculations. It has been shown that a complex FFT measurement has $4N - 2log_2{}^2N - 2log_2N - 4$ real-valued multiplications [15] and $O(N \log N)$ complex-valued additions [16]. Each complex-valued addition has two real-valued additions: one for the real part and the other for the imaginary part. Assuming large values of N, we approximate the value of M per measurement sample for the Complex FFT Spectrum to be $4 + 2 * log_2 2$. The final measurement being compared is the Angle of Arrival Measurements used in beam steering and beam forming applications. The value of M for this measurement is calculated using $a^2 * N$ number of multiplications and $a^2 * (N - 1)$ number of additions [17], where a is the number of antenna elements, and N is the number of samples. In this work, we assume that the number

of antenna elements is set to 16. Using these values, M is set to 256 per measurement sample.

4.2 Results and Observations

Table 4 shows the time taken (in microseconds) by each measurement on the three different testbed architectures, using the values of M as calculated above and the other parameters as shown in Tables 1, 2, and 3.

Table 4: Time (in microseconds) for each measurement on different testbed architectures, $k = 0.3$ for PB

Measurement	GP	PB	mmMoReEdge
IQ Power	2.16	0.66	0.33
FFT	4.82	1.23	0.50
AoA	195.2	43.17	13.06

In this table, the value of k is assumed to be 0.3, which implies that only 30% of the FPGA resources are available for measurement, while the rest of the FPGA fabric is being used for hardware configuration. This is only applicable for the PB testbed. As demonstrated by the results, the proposed mmMoReEdge testbed outperforms the other two architectures for all the three cases. We observe that, while the speedup is marginal for low-complexity measurements (such as IQ Power), it increases significantly as the complexity of the measurement increases. Figure 3 shows how the measurement

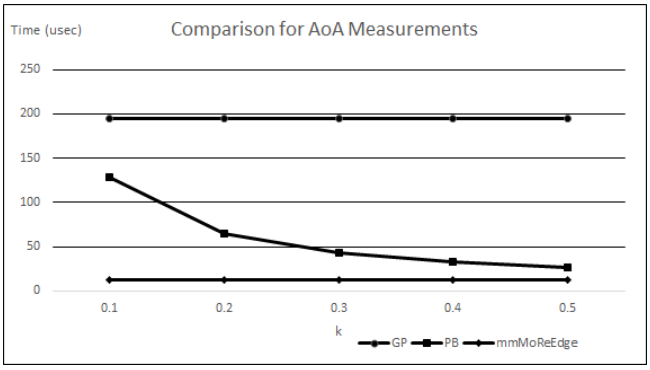

Figure 3: Comparision of AoA measurements with different values of K

time varies as a function of k for the Angle of Arrival measurement. We choose to present this measurement because it is the most complex of the three measurements. We vary values of k from 0.1 to 0.5, based on the assumption that, even in the best case, at least 50% of the FPGA resources will be used for hardware configuration. In other words, only 50% of the resources will be available for measurements. Changing the value of k does not have an impact on the measurement times for GP and mmMoReEdge because these architectures do not rely on the FPGA on the node for processing.

Figure 4 shows the performance comparison between PB for two values of k and mmMoReEdge, using the general purpose architecture as a baseline. Performance improvement P, as a percentage, is measured using Equation 3.

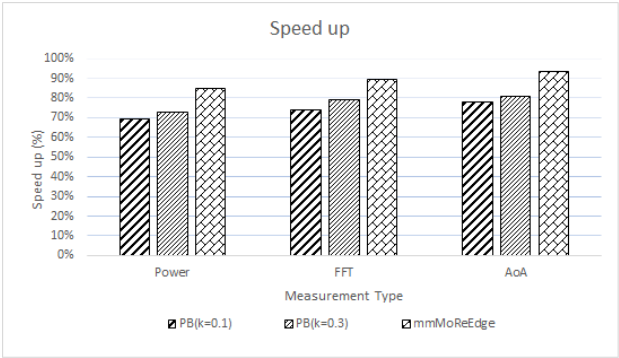

Figure 4: Speedup Comparison using GP as baseline

$$P = \mid t_{gp} - t_i \mid / t_{gp} * 100, t_{gp} > 0 \quad (3)$$

Here, t_{gp} is the time taken for the measurement on a testbed with the general purpose architecture, and t_i is the time taken for the measurement on a testbed with the architecture being compared. In particular, the proposed mmMoReEdge design and the programmable blocks architectures have values of $k = 0.3$ and $k = 0.1$. Our results indicate that mmMoReEdge is around $85\% - 93\%$ faster than the GP architecture, and the performance improvements are more pronounced as the complexity of the measurements increases. For $k = 0.3$, the proposed design is 50% faster for the IQ Power measurements, whereas it is 70% faster for the Angle of Arrival measurements.

5 RELATED WORK

Existing 5G testbeds have been designed to meet the requirements of a specific application or achieve a particular learning outcome. They have been primarily designed for conductive (or cabled) stationary measurements and then, in some cases, adapted for mobile applications. The 5G CHAMPION testbeds [18] were designed for the 2018 Winter Olympic games to validate how 5G-enabled mmWave wireless backhaul can provide an inter-operable and seamless connection between two different access networks. The 5G Hardware Test Evaluation Platform [19] deploys software-defined wireless networks in an urban area, allowing academics, entrepreneurs, and wireless companies to test, evaluate, and improve their hardware design and software algorithms in a real-world environment. An approach focused on an educational setup for service-oriented process automation with 5G for emerging industrial technologies can be found in [20]. One testbed demonstrates SDN orchestration capabilities in adapting data paths across IoT, cloud, and network domains, based on the real-time load state of switches [21], enabling recovery from congestion, and assuring reliable data-delivery services. Each of these platforms have a high degree of specificity as to which applications they are built but less programmable than researchers might ultimately desire. POWDER [22] and COSMOS [23] projects, funded through the NSF PAWR initiative, are promising as they have been proposed emerging ideas for emerging mmWave frequency bands, different applications, and evolving specifications.

Our work is an effort to take inspiration from the edge computing architectures on IoT devices and apply it for a modular and reconfigurable 5G testbed.

6 CONCLUSION

5G focuses on various aspects of present-day communication challenges such as area traffic capacity, network energy efficiency, connection density, and latency but also looks to the future of cellular networks, which must focus on spectrum efficiency and mobility. As a result, 5G is a prime candidate for emerging health, energy, public safety, and transportation applications. This paper addresses a key area of need in the long-term adoption of this standard for these applications by presenting the design of mmMoReEdge, a modular and reconfigurable testbed based on an edge computing architecture. A mathematical model for processing time as the key metric is presented to evaluate different testbed architectures. Three different use cases are described as examples of low, medium, and high complexity measurements, typically found in 5G test scenarios. The simulation results show that mmMoReEdge is 50% to 70% faster as compared to an offline CPU-based architecture and is 30% to 40% faster as compared to a node-based architecture with one FPGA.

7 APPENDIX

This code calculates the processing time for each of the three measurements, namely power measurements, complex FFT spectrum, and Angle of Arrival (AoA) on the GP, PB, and MoreEDGE testbed architectures. Code is written in Python 3.6.2. To generate the results shown in Table 4, Figure 3, and Figure 4, run the following program.

```
import math
#Generic constants
N=1024 #number of samples
B=[1e9, 2.5e9, 4e9]
P=[2.7e9, 40e6, 40e6]
t=[0, 0, 0]
k=[1, 0.3, 1]
tmp=0.0
m=[]



##number of operations for IQ Power
m.append(3)
#number of operations for Complex FFT
m.append(4+2*math.log(N,10.0))
#number of operations for AoA
m.append(16*16*2)
meas=["IQ Power", 'FFT Spectrum', 'AoA']
print("Results for Table 4")
#outer loop for measurements
for j in range(3):
    t=[0,0,0]
    #inner loop for number of processors
    for i in range(3):
        if i == 0:
            s=[1024, 0, 0]
            M=[m[j]*N, 0, 0]
        elif i == 1:
            s=[1, 1024, 0]
            M=[0, m[j], 0]
        elif i == 2:
            s=[1, 1, 1024]
            M=[0, 0, m[j]]
        else: print("Error Condition")
        t1=(s[i]/B[i])
        t2=((M[i]/(P[i]*k[i])))
        t[i]+=(t1+t2)/1e-6
    print("--------------------------------")
    print("|", meas[j],
          "|", format(t[0],'.2f'),
          "|", format(t[1],'.2f'),
          "|", format(t[2],'.2f'),
          "|")
    print("--------------------------------")
print("------------------------------------")

print("Results for Figure 3, PB graph")
k=[0.1, 0.2, 0.3, 0.4, 0.5]
t=[0,0,0,0,0]
#outer loop for k
for j in range(5):
    #inner loop for number of processors
    for i in range(3):
        s=[1, 1024, 0]
        M=[0, m[2], 0]

        t1=(s[i]/B[i])
        t2=((M[i]/(P[i]*k[j])))
        t[j]+=(t1+t2)/1e-6

print("------------------------------------")
print("|", format(t[0],'.2f'),
      "|", format(t[1],'.2f'),
      "|", format(t[2],'.2f'),
      "|", format(t[3],'.2f'),
      "|", format(t[4],'.2f'),
      "|")
print("------------------------------------")
```

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