Preliminary Information

• Instructor Introduction
• Class Policies
  – Disabilities/Religious Holidays
  – Cheating/Copying
• Class Web Site
  – Class Notes
  – Class Schedule
  – Laboratories
  – Personal Installation of Class Software
    • Some Available
    • MUST USE LABORATORY INSTALLATION FOR LAB DEMONSTRATIONS/GRADING!!

Previous Courses

• Digital Logic Design
  – Boolean Algebra
  – Simple Combinational, Sequential Networks (< 100 gates/memory elements)
  – TTL, PLD implementation technologies
  – CAD Experience Recommended: Intro HDL
• Microprocessors/Assembly Language
  – Instruction sets, basic architecture
  – Assembly language programming
  – Microprocessor based solutions for Digital control
CSE/EE 5387/7387 Digital Systems Design

• Moderate Sized Combinational and Sequential networks
  (~ thousands of gates/memory elements)
  – Emphasis on combined datapath+Finite synchronous state machine designs for high performance applications
  – arithmetic circuits+controllers
• CAD tool usage (schematic entry, simulation, synthesis, technology mapping, timing analysis)
• Logic Synthesis via HDLs (Verilog/VHDL)
• Implementation Technology: Field Programmable Gate Arrays (FPGAs)

Course Philosophy

• Reese/Thornton and Davis/Reese booklets followed
• Brown/Vranesic textbook in this course is more of a reference
  – Will help, especially with logic synthesis
• Material in class based on instructor notes
  – Most notes online, see both:
    lyle.smu.edu/~dhougninou
    Especially look at the CLASS SCHEDULE Page
• You will need to stay caught up on lecture material. Falling behind is difficult to recover from.
Moore’s Law

source: intel.com

SIA Roadmap Estimate

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MOSFET Structure
Metal Oxide Semiconductor Field Effect Transistor

Continuous Range of Energy Levels within the Channel

source: Scientific American

Feature Size Trend
Feature Size Trend

![Graph showing feature size trend with specific data points and lines indicating technology nodes.

Si Wafer

Figure 1.1  A silicon wafer
AMD Typhoon 45 nm

- Demonstrated May 09, 2007

Power Requirements

Power Density Extrapolation

Design Target Technology

- Standard Components
- Custom and Semi-custom
- Emerging Technology
- Programmable Logic

Standard Components

- Example: 74XX Components
- Commonly Used Logic Functions
- Less Than 100 Transistors
- Common ones Used in Previous Class
- Not Used Currently as They Use Too Much Board Area
Application Specific ICs (ASICs)

• Not a Fixed Internal Architecture
• Expensive to Design
• Variety of Techniques-Std. Cell to Full Custom
• Best in Terms of Area/Performance/Power

Nano and Quantum Devices

EMERGING TECHNOLOGY

Solid State Devices

CMOS Devices

Nano CMOS
Very Small Feature Size

CNFET
Carbon Nanotube FET

Quantum Devices (bulk effect)

Quantum Dot

RTD
Resonant Tunneling Diode

SET
Single Electron Transistor

Molecular Devices

Electrochemical

Photoactive

Electromechanical

Quantum Effect

Programmable Logic Devices

- Flexibility Allows More Complex Function Realization than 74XX Chips
- Can Be Reprogrammable
- Modern State of Art is ~100 Million Transistors
- Becoming Increasingly More Common in Target Design
- Important use in ASIC Hardware-assisted Emulation

Typical Programmable Device

Figure 1.2 A field-programmable gate array chip
Figure 1.3  The development process

Figure 1.4  The basic design loop

Design Flow with Validation (not just Functional Correctness)
Figure 1.6  Design flow for logic circuits
Course Software

• We will Primarily use Altera Quartus2
• Altera Quartus2 PC version available
  – Course Webpage has link to Altera site for software
  – Use On-campus Installations for Demonstrations
  – Other Prog. Logic Software:
    • Synopsys Synplicity and VCS
    • Cadence Verilog Simulator
    • Altera QuartusII
    • Xilinx Tools

Required Course Software

- Schematic Capture (Altera)
- Design Specification
- Manual HDL Generation
- Auto. HDL Generation (Altera)
- HDL Simulation (Altera)
- FPGA Synthesis (Altera)
Course Software (cont)

• Software is the same as used by practicing engineers in industry.
• **HIGHLY RECOMMEND** that you install it on your home PC
• Work on your Lab **BEFORE** your lab session
• Permissible to have Lab Completed Ahead of Time Then Demonstrate Only During Lab Period
• Lab Period is YOUR Time to get Debugging Help with Your Design

Lecture, Labs

• Lecture is Mon.-Wed.
• Attend your lab session
  – to hear explanation of lab assignment
  – to get help debugging
  – Can complete assignment on home PC. Upload files from home for TA checkoff.
• Lab assignments due during your assigned lab time unless otherwise noted.
Altera Quartus2 Tutorial

• This is a short tutorial on Altera tools schematic capture and simulation
• You have the choice of using either the PCs in Lab or your PC.
  – I would suggest Lab PCs; you can get help if you need it!
  – Files created under the PC version are compatible with the Unix version and vice-versa.
  – We do Have Altera Available on the UNIX Machines (only 1 license though – NOT RECOMMENDED!)
QuartusII Tools Menu

Compile/Map schematic/HDL to FPGA
Simulate Design
Analyze Timing of Mapped design
View Placed/Routed Chip – minor changes
Allows View of Schematic at RTL Level
Built-in LA for Actual Devices
Download design to FPGA

Our Design Methodology

Create/Edit Schematic/HDL
Compiler
repeat until no errors
Create Simulation Waveforms
Simulator
Run simulation until design is validated
Timing Analysis?
Modify design until timing specs met.
Program Device
File Types (QuartusII)

- .bdf - Device design files or schematics
- .v - Verilog files
- .vwf - Waveform files
- .rpt - Report files. (Note that there are multiple report files)
- .qpf and .qsf - Project files
- .bsf - Block symbol file

There are MANY other files automatically generated by various tools. Only the **above types (.bdf, .v) need to be preserved** in order to keep your design; the other files can be deleted.

File Creation

To create any new file, use File -> New command from main menu, will pop up file creation menu, choose a type.
After creating schematic or HDL file, clicking on start button will start compilation process. After compilation is complete, can simulate design (if you have created a test waveform for the design).

For more detailed instructions

- Lab #0 has more detailed instructions in its writeup
- Experiment with different menu choices
- Refer to online help
- Ask the Lab Instructor
A sample schematic is shown below for reference.