FPGA Timing Models

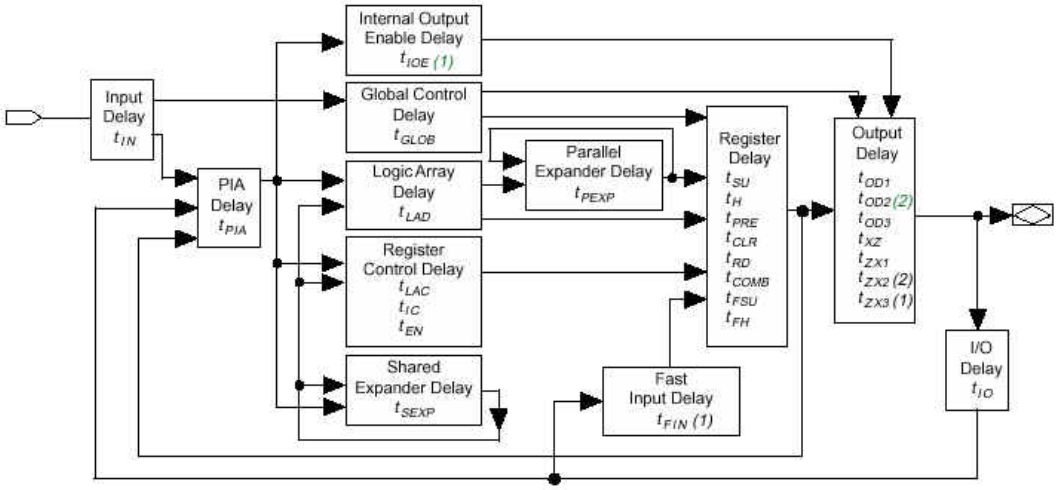
- Many FPGA and CPLD vendors provide a *timing model* in their data sheets that allow estimation of path delays.
- Some example path delays that are of interest:
  - Minimum Pin to Pin (combinational) delay
    - (through input pin, through one combinational logic element, through one output pin.)
  - Minimum Register to Register Delay
    - From clock input pin, through global net . through Clock to Q delay through DFF of a logic element, through one combinational logic element to setup time on DFF input).

FPGA Timing Models (cont)

- These timing models allow estimates of maximum attainable performance
- Some vendors use their timing models as selling points
  - Simpler is better - easier to estimate timing from a simple model than a complex one.
  - Routing delays will always complicate the timing model
- After a design is mapped to an FPGA or CPLD, use a static timing analysis program to estimate the timing performance.

Altera M7000 Timing Model

Figure 12. MAX 7000 Timing Model



Notes:
(1) Only available in MAX 7000E and MAX 7000S devices.
(2) Not available in 44-pin devices.

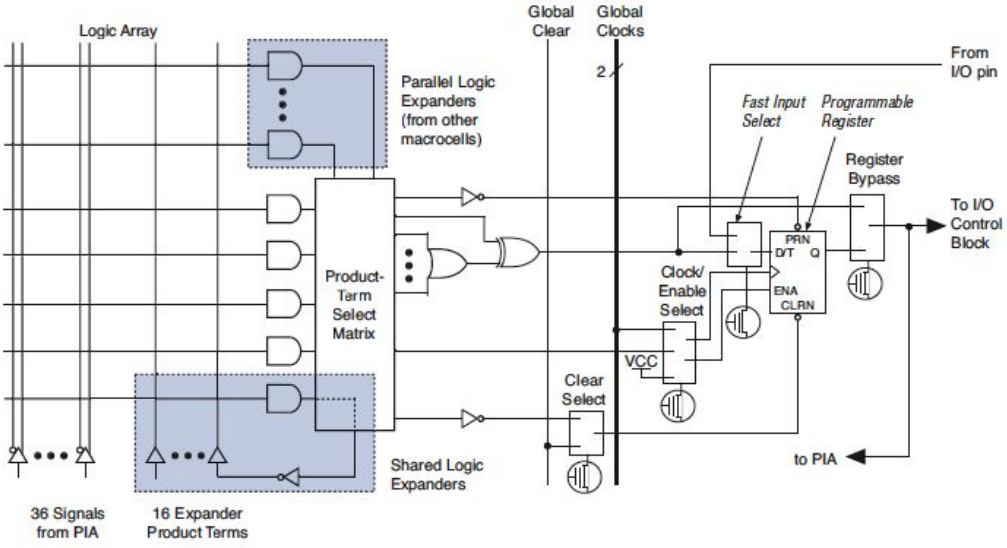
Altera M7000 Timing Defns

Table 16. MAX 7000 & MAX 7000E External Timing Parameters Note (1)

Symbol	Parameter	Conditions	Speed Grade				Unit
			-6		-7		
			Min	Max	Min	Max	
t_{PD1}	Input to non-registered output	C1 = 35 pF		6.0		7.5	ns
t_{PD2}	I/O input to non-registered output	C1 = 35 pF		6.0		7.5	ns
t_{SU}	Global clock setup time		5.0		6.0		ns
t_{H}	Global clock hold time		0.0		0.0		ns
t_{FSU}	Global clock setup time of fast input	(2)	2.5		3.0		ns
t_{FH}	Global clock hold time of fast input	(2)	0.5		0.5		ns
t_{CO1}	Global clock to output delay	C1 = 35 pF		4.0		4.5	ns
t_{CH}	Global clock high time		2.5		3.0		ns
t_{CL}	Global clock low time		2.5		3.0		ns
t_{ASU}	Array clock setup time		2.5		3.0		ns
t_{AH}	Array clock hold time		2.0		2.0		ns
t_{ACO1}	Array clock to output delay	C1 = 35 pF		6.5		7.5	ns
t_{ACH}	Array clock high time		3.0		3.0		ns
t_{ACL}	Array clock low time		3.0		3.0		ns
t_{CPPW}	Minimum pulse width for clear and preset	(3)	3.0		3.0		ns
t_{ODH}	Output data hold time after clock	C1 = 35 pF (4)	1.0		1.0		ns
t_{CNT}	Minimum global clock period			6.6		8.0	ns
f_{CNT}	Maximum internal global clock frequency	(5)	151.5		125.0		MHz
t_{ACNT}	Minimum array clock period			6.6		8.0	ns
f_{ACNT}	Maximum internal array clock frequency	(5)	151.5		125.0		MHz
f_{MAX}	Maximum clock frequency	(6)	200		166.7		MHz

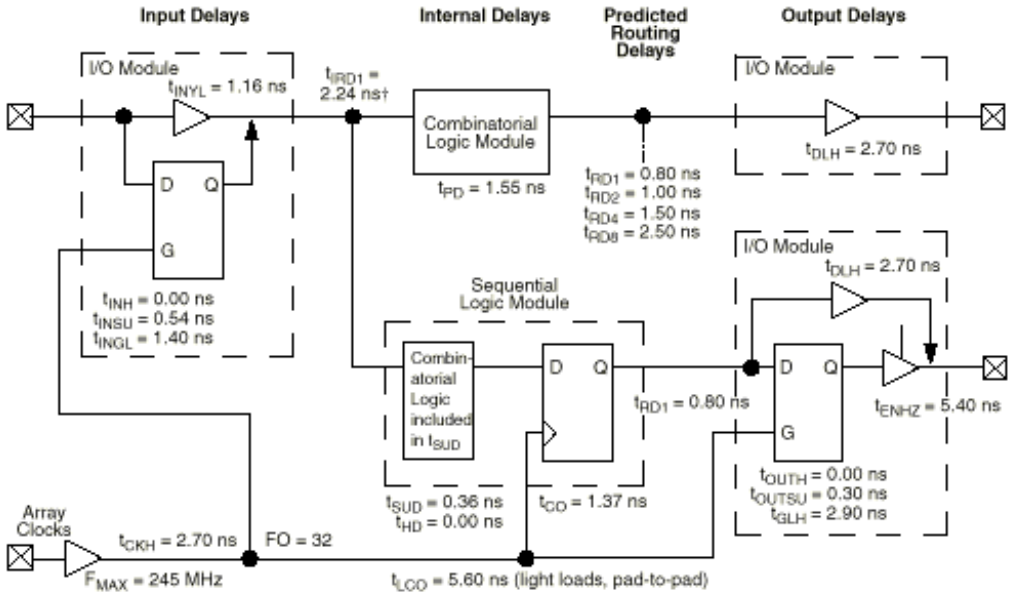
Altera M7000E Logic Element

Figure 3. EPM7032, EPM7064 & EPM7096 Device Macrocell



Actel 42MX Timing Model

42MX Timing Model*



*Values are shown for A42MX09-2 at 5.0V worst-case commercial conditions † Input module predicted routing delay

Comb. Pin to Pin delay Example

Input pad through combinational element through output pad

From timing model:

T_{INYL} + T_{IRD1} + T_{PD} + T_{RD1} + T_{DLH}

1.16ns + 2.24 ns + 1.55ns + 0.8 ns + 2.7 ns

Pin to Pin = 8.45 ns

T_{INYL} Input pad to Y low
T_{IRD1} Input Fanout 1 routing delay (higher the fanout, longer the delay)
T_{PD} Logic module prop delay
T_{RD1} Output Fanout 1 routing delay
T_{DLH} Data to Pad high delay

Environment affects Timing

Actel uses derating factors for timing values. A derating factor is a multiplication factor applied to the timing value.

42MX Temperature and Voltage Derating Factors
(Normalized to T_J = 5V, 25 °C)

42MX	–55	–40	0	25	70	85	125
4.50	0.93	0.95	1.05	1.09	1.25	1.29	1.41
4.75	0.88	0.90	1.00	1.03	1.18	1.22	1.34
5.00	0.85	0.87	0.96	1.00	1.15	1.18	1.29
5.25	0.84	0.86	0.95	0.97	1.12	1.14	1.28
5.50	0.83	0.85	0.94	0.96	1.10	1.13	1.26

Notice that fastest timing (smallest derating factor) is for high Voltage, low temperature. The slowest timing (largest derating factor) is for low voltage, high temperature.

Four corners: (low temp, low Vdd), (high temp, low Vdd), (low temp, high Vdd), (high temp, high Vdd).

Processing Variations can also affect Timing

Timing can vary from one batch of wafers to another due to process variations. There are also *four corners* for processing variations: (fast-p, fast-n), (slow-p, fast-n), (fast-p, slow-n), (slow-p, slow-n). 'fast-p','slow-p' refer to fast PMOS transistors, slow PMOS transistors. 'fast-n', 'slow-n' refer to fast NMOS transistors, slow NMOS transistors, respectively.

Data sheets use timing variations due to processing to determine the speed grades; Voltage/Temperature derating factors are then applied to individual speed grade timings.

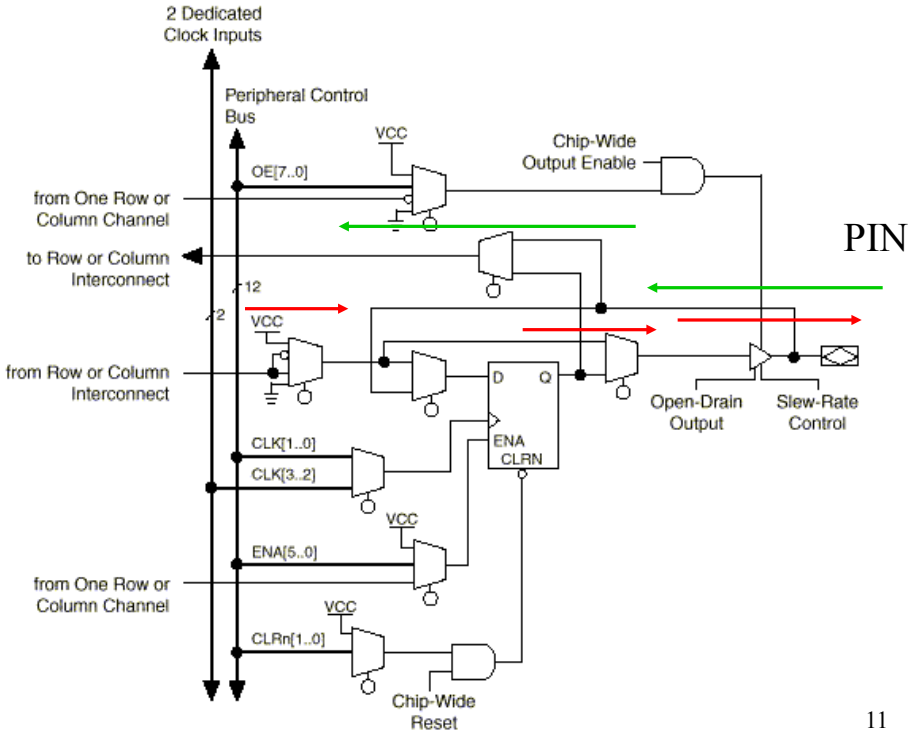
Actel specifies a 0.45 derating factor for best case processing. This would be important if you were trying to compute the minimum delay.

Speed Grades

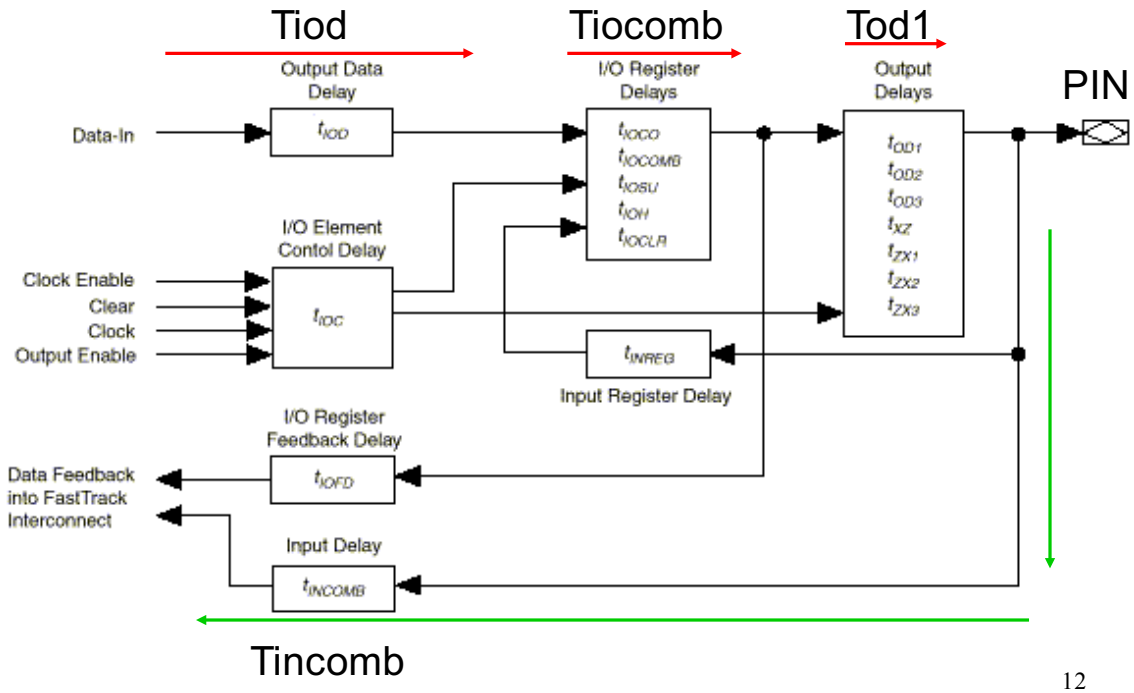
- Important to realize that speed grades are determined via the timing variations due to processing
  - There are no functional differences between speed grades.
  - A functional difference would require a different part number.
- Vendors will charge premium prices for the best speed grade parts

Altera IO Element

Logic Element array



Altera IOE Timing model



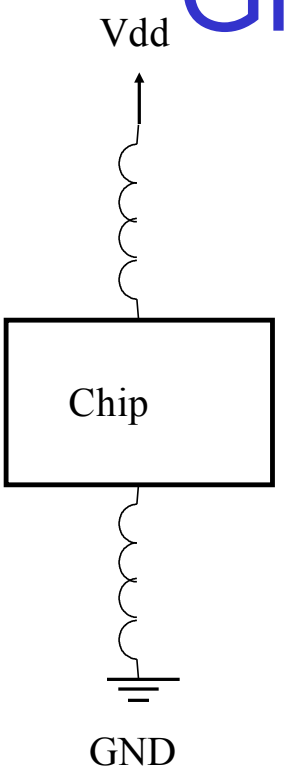
IOE (I/O Element) Delays

- Input path
  - Tincomb - input pad and buffer to fasttrack interconnect delay
- Output path (combinational path with fast output slew)
  - Tiod - data delay
  - Tiocomb - combinational delay
  - Tod1 - slow rate = off, Vccio = Vccint (Vcc of IO pad is same as internal Vcc).

Aside: Why programmable Output slew?

- Slew rate is the measure of how fast an output can change value (measured in Volts/Sec).
- Most FPGA vendors offer the capability of programming the output to be either fast slew or slow slew ----- WHY?
  - Fast Slew rates cause more noise problems via ground bounce, especially when multiple outputs are switching
  - If you have room in your timing spec, should use slow slew rate if possible

GND Bounce



Large change of current on Vdd/Gnd pins (inrush current) due to multiple outputs changing simultaneously causes induced voltage on GND plane:

$$v(t) = L * di/dt$$

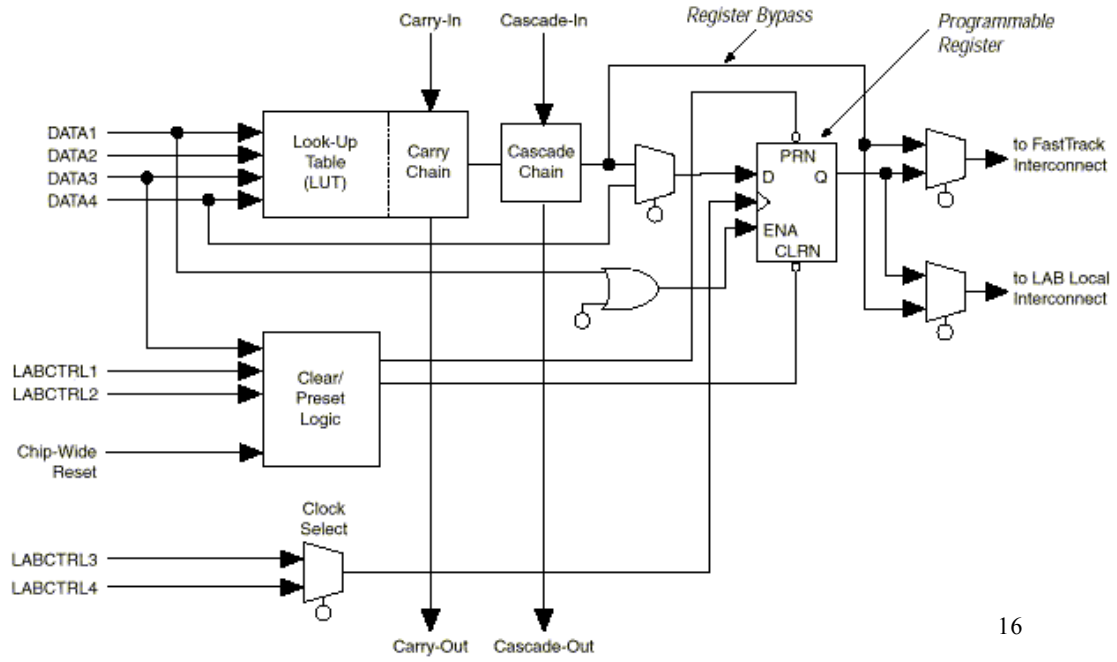
Larger the inductance, larger the change in current, larger the induced voltage.

Two ways to reduce Voltage:
Reduce Inductance : More Vdd/gnd pins (inductance in parallel reduces total inductance), better packaging (different packages have more/less inductance than others).
Flex 10K20 240 pin package has 19 Vdd pins, 18 Gnd pins).

Reduce di/dt : slower slew rate!!!!

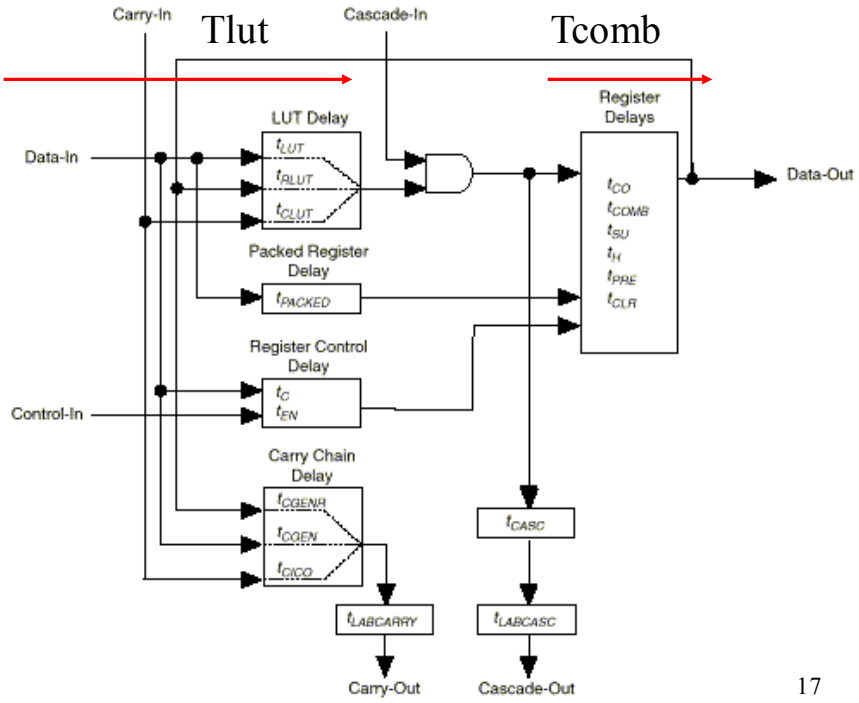
Altera Logic Element

Figure 6. FLEX 10K Logic Element



Altera Logic Element

Figure 23. FLEX 10K Device LE Timing Model



Minimum Combinational Pin To Pin Delay

[Input Pin delay] + [Logic Element Delay] + [Output Delay]

[Tincomb] + [Tlut + Tcomb] + [Tiod + Tiocomb + Tod1]

What about Routing Delays? Table 36 & 44 (in data book) has routing delays.

Tdin2data - delay from dedicated input or clock to LE data

Tsamecolumn - delay from LE output to IOE in same column

Tsamerow - delay from LE output IOE in same row

Minimum Combinational Pin To Pin Delay

[Input Pin delay] + [Routing] + [Logic Element Delay] + [Routing] + [Output Delay]

[Tincomb] + [Tdin2data] + [Tlut + Tcomb] + [Minimum (same col,row)] + [Tiod + Tiocomb + Tod1]

[3.1] + [4.3] + [1.4 + 0.5] + min(0.9,3.6) + [1.3 +0.0 + 2.6]

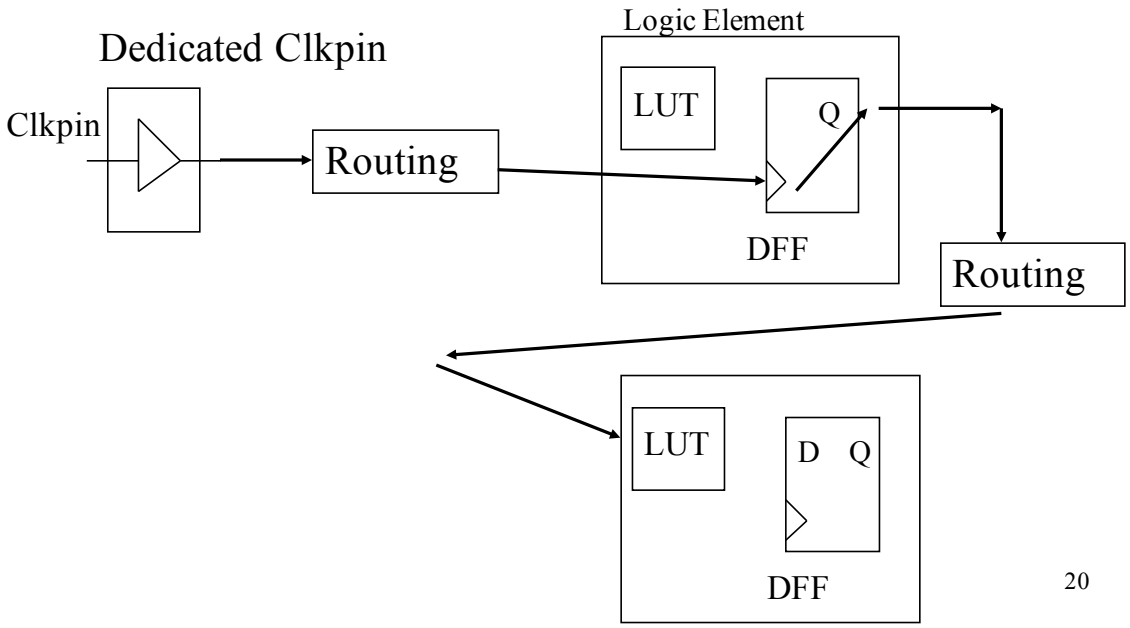
= 14.1 ns

if ignore routing, then 8.9 ns (**this is what marketing may quote in datasheets**).

Note that same column routing much faster than row routing (hence dedicated carry chains run in column routing).

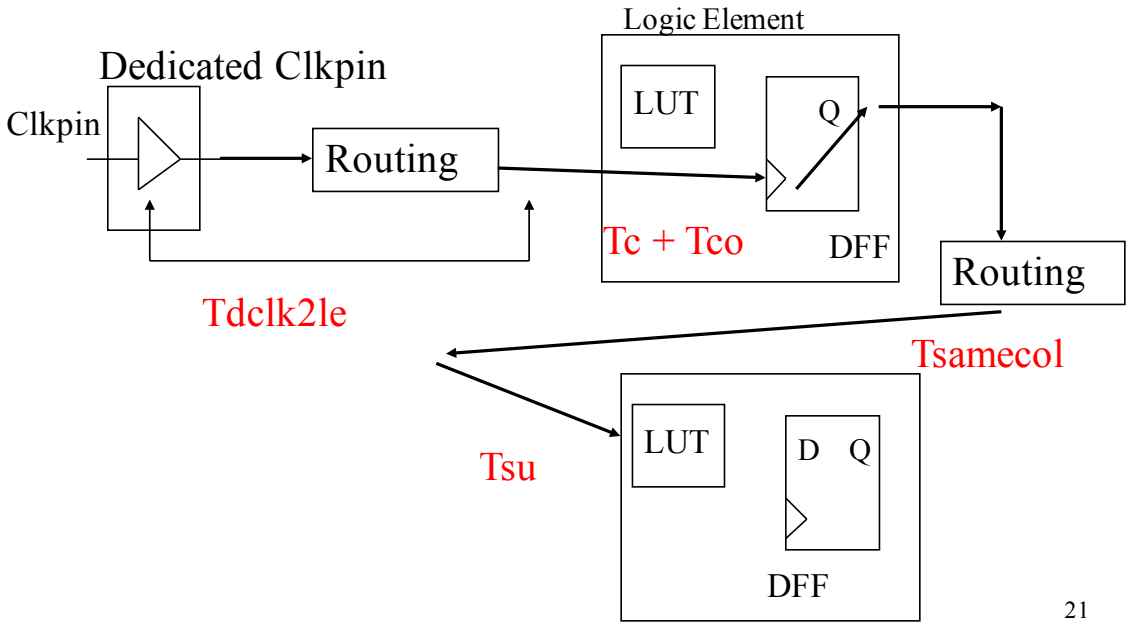
Minimum Clock to Register

[Input Pin delay] + [Routing] + [Logic element clock-to-Q] + [Routing] + [Logic Element Delay] + [Routing] + [Logic Element Setup Time]



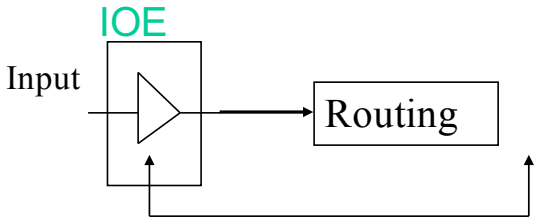
Minimum Clock to Register

[Input Pin delay] + [Routing] + [Logic element clock-to-Q] + [Routing] + [Logic Element Setup Time]

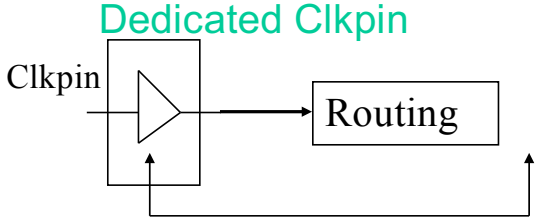


Dedicated Inputs/Clock Pins vs IOE inputs

A dedicated input pin or dedicated clock pin does not have the IOE logic. The input timing is specified as routing delay only:



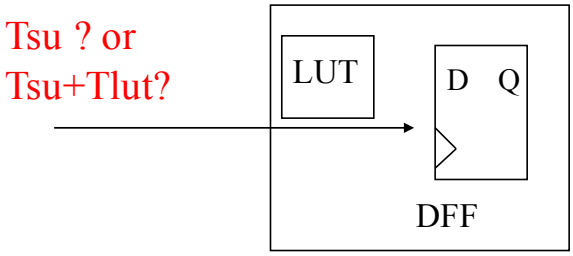
Tincomb + Tsamecol = 3.1ns + 1.4ns = 4.4 ns



Tdclk2le = 2.6 ns

Use dedicated input pins to minimize input delay. Not many on device - 10K20 240 pin package only has 4 dedicated inputs and 2 dedicated clock pins.

Setup Time for Logic Element

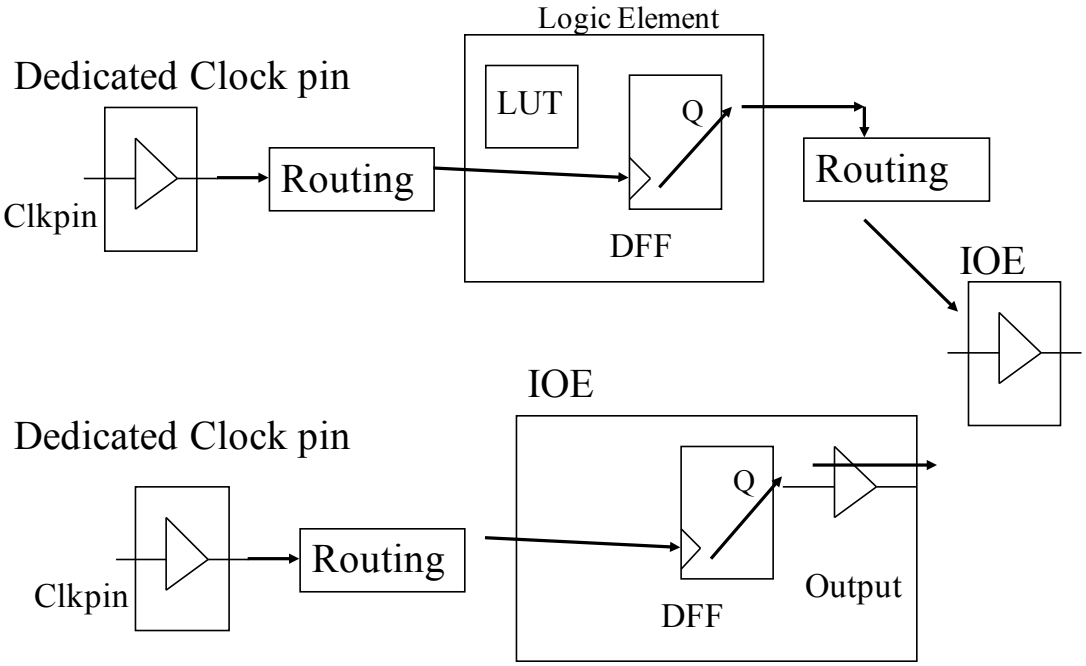


Typically, the setup time specification for an external data input already accounts for the LUT delay since the data input has to pass through the LUT on its way to the D input.

The Altera spec is a bit confusing - my best guess is that Tsu includes the LUT delay. There is no doubt that the Xilinx Virtex Tsu spec includes the LUT delay.

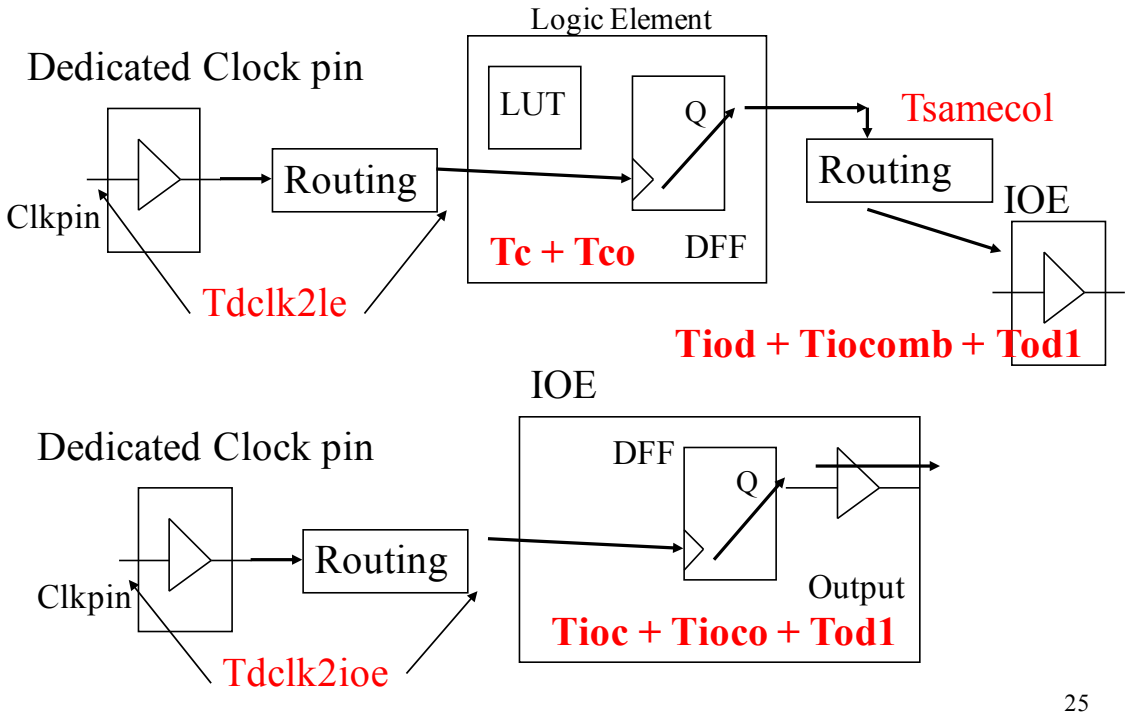
Clock To Out

Two different Choices here - is the Dff in the LUT or the IOE??



Clock To Out

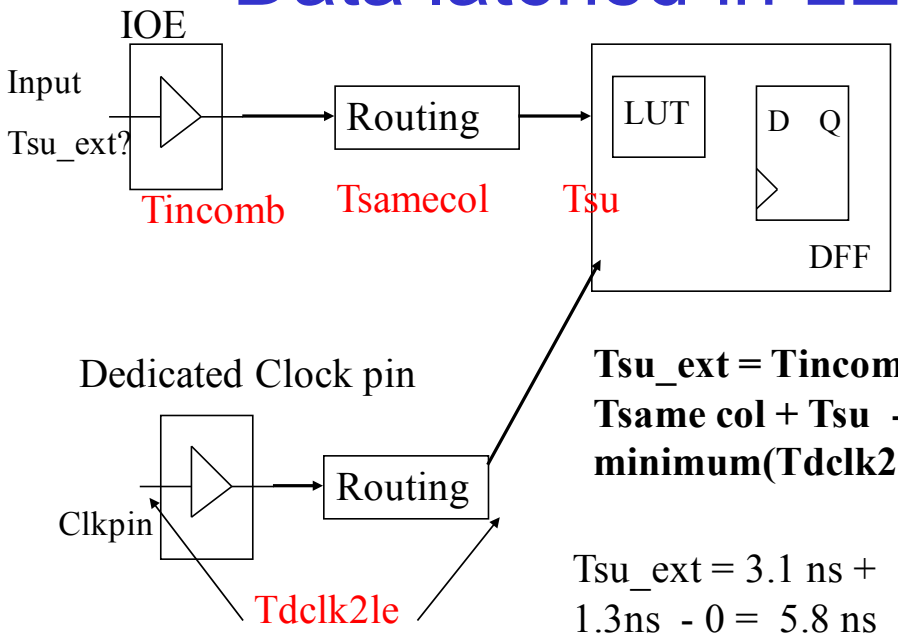
Two different Choices here - is the Dff in the LUT or the IOE??



Latching in I/O Element or Logic Element?

- The DFF in the IOE can be configured to either latch incoming data or outgoing data
  - Can latch ingoing/outgoing data in either IOE or LE (logic element)
- Using the DFF in the IOE to latch outgoing data will usually reduce Clock-2-Out time
  - DFF is closer to the Pin!
- Using the DFF in the IOE to latch ingoing data will reduce external setup time.
  - DFF is closer to the Pin!

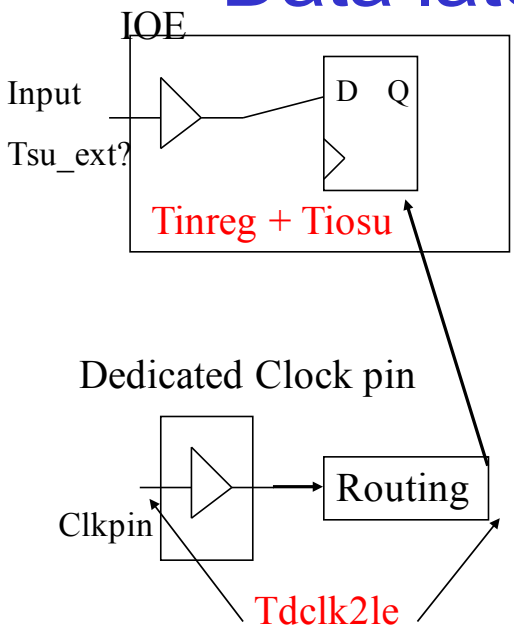
Minimum External Setup Time Data latched in LE



Tsu_ext = Tincomb + Tsame col + Tsu - minimum(Tdclk2le)

Tsu_ext = 3.1 ns + 1.4ns + 1.3ns - 0 = 5.8 ns

Minimum External Setup Time Data latched in IOE

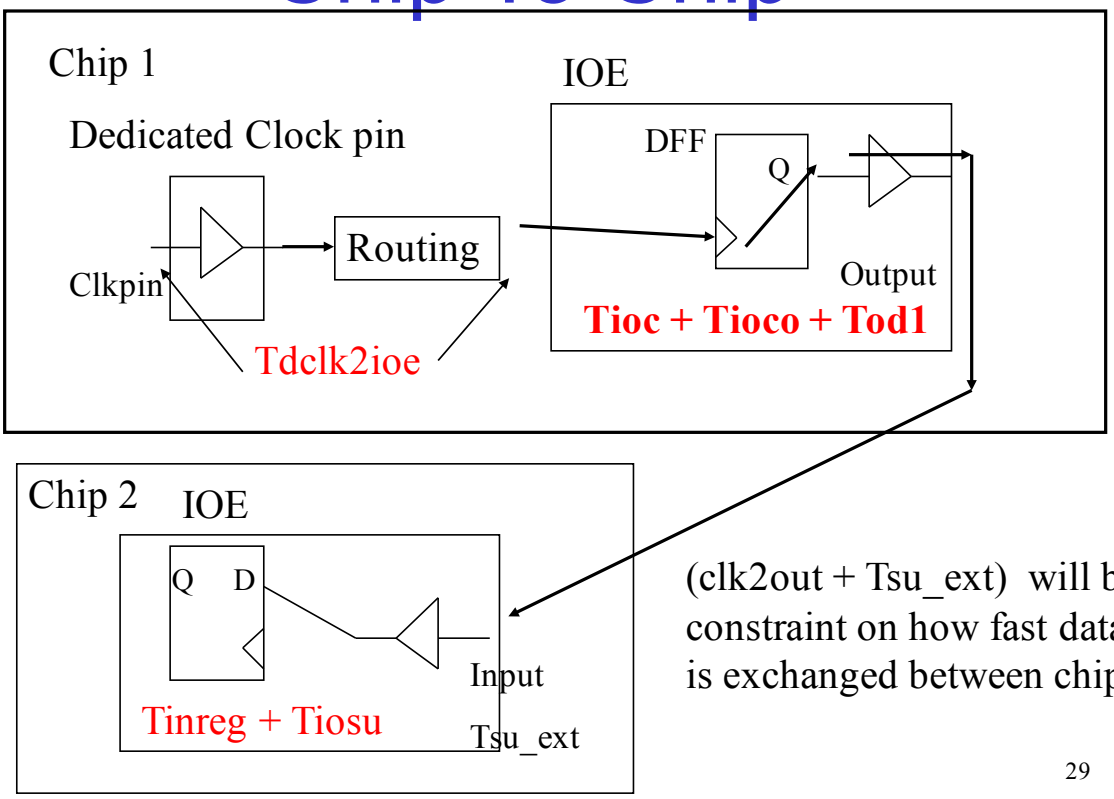


Tsu_ext = Tinreg + Tiosu - minimum(Tdclk2le)

Tsu_ext = 6.0 ns + 2.8 - 0 = 8.8 ns

!! Latching in IOE slower than in Logic Element? These are all worse case numbers in the datasheet which could account for this; also mentioned on page 28 that latching in LE element will sometimes give better setup time than an IOE. For other FPGA families this is usually not the case.

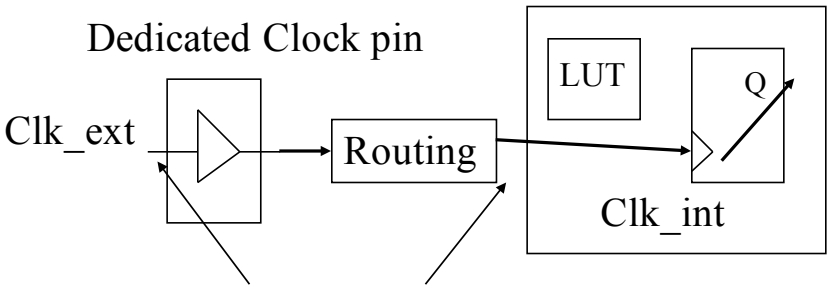
Chip To Chip



(clk2out + Tsu_ext) will be constraint on how fast data is exchanged between chips

PLL effects

PLL/DLL will synchronize internal clock to external clock. Aim is to have zero delay between clock edges at Logic elements and external clock edge



Want a 'zero-delay' clock, no difference in edge arrival times of clock edges at 'Clk_ext' and 'Clk_int'.

Overall Device Features
Altera M7000 Series

Table 1. MAX 7000 Device Features

Feature	EPM7032	EPM7064	EPM7096	EPM7128E	EPM7160E	EPM7192E	EPM7256E
Usable gates	600	1,250	1,800	2,500	3,200	3,750	5,000
Macrocells	32	64	96	128	160	192	256
Logic array blocks	2	4	6	8	10	12	16
Maximum user I/O pins	36	68	76	100	104	124	164
t_{PD} (ns)	6	6	7.5	7.5	10	12	12
t_{SU} (ns)	5	5	6	6	7	7	7
t_{FSU} (ns)	2.5	2.5	3	3	3	3	3
t_{CO1} (ns)	4	4	4.5	4.5	5	6	6
f_{CNT} (MHz)	151.5	151.5	125.0	125.0	100.0	90.9	90.9

Altera Operating Requirements

- Absolute Maximum Ratings
  - Stress Ratings, Values outside this area will permanently damage device
- Recommended Operating Conditions
  - Voltage Ranges for Safe Operation
- DC Operating Conditions
  - Steady-state Expected Values for Currents and Voltages
- AC Operating Conditions
  - Internal/External Timing Parameters
  - Assume Operation at DC Operating Conds.

DC Operating Conditions

- V_{IH} - Input Voltage Sensitivity (Logic – High)
- V_{IL} - Input Voltage Sensitivity (Logic – Low)
- V_{OH} - Output Voltage Typical (Logic – High)
- V_{OL} - Output Voltage Typical (Logic – Low)
- I_{OH} - Output Current Drive (Logic – High)
- I_{OL} - Output Current Drive (Logic – Low)
- I_I - Input Current Leakage
- I_{OZ} - Output Current Leakage

Altera M7000 Absolute Maximum

Table 10. MAX 7000 5.0-V Device Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to ground *(2)*	–2.0	7.0	V
V_I	DC input voltage		–2.0	7.0	V
I_{OUT}	DC output current, per pin		–25	25	mA
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–65	135	° C
T_J	Junction temperature	Ceramic packages, under bias		150	° C
		PQFP and RQFP packages, under bias		135	° C

Altera M7000 Recommended Op. Ranges

Table 11. MAX 7000 5.0-V Device Recommended Operating Conditions

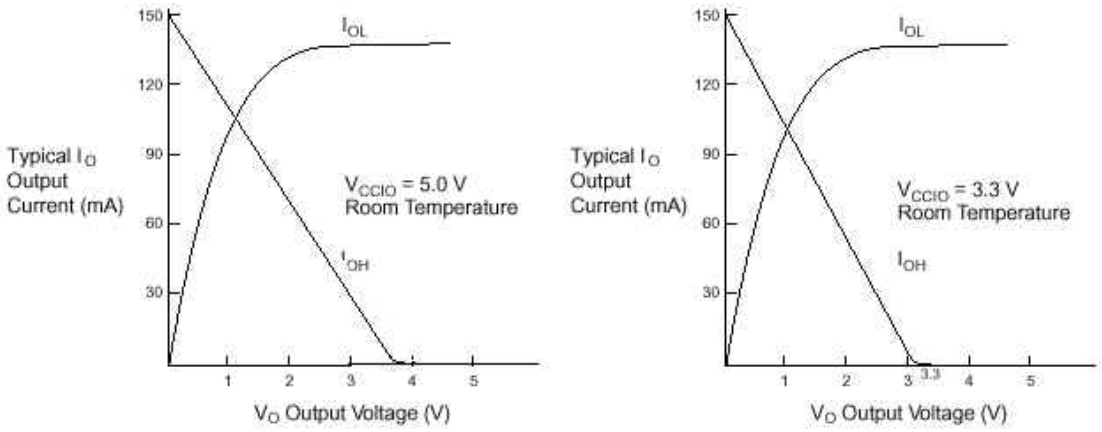
Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers	*(3), (4)*	4.75 (4.50)	5.25 (5.50)	V
V_{CCIO}	Supply voltage for output drivers, 5.0-V operation	*(3), (4)*	4.75 (4.50)	5.25 (5.50)	V
	Supply voltage for output drivers, 3.3-V operation	*(3), (4), (5)*	3.00 (3.00)	3.60 (3.60)	V
V_{CCISP}	Supply voltage during ISP	*(6)*	4.75	5.25	V
V_I	Input voltage		–0.5 *(7)*	V_{CCINT} + 0.5	V
V_O	Output voltage		0	V_{CCIO}	V
T_A	Ambient temperature	For commercial use	0	70	° C
		For industrial use	–40	85	° C
T_J	Junction temperature	For commercial use	0	90	° C
		For industrial use	–40	105	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

Altera M7000 DC Op. Conds.

Table 12. MAX 7000 5.0-V Device DC Operating Conditions *Note (8)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	High-level input voltage		2.0	V_{CCINT} + 0.5	V
V_{IL}	Low-level input voltage		–0.5 *(7)*	0.8	V
V_{OH}	5.0-V high-level TTL output voltage	I_{OH} = –4 mA DC, V_{CCIO} = 4.75 V *(9)*	2.4		V
	3.3-V high-level TTL output voltage	I_{OH} = –4 mA DC, V_{CCIO} = 3.00 V *(9)*	2.4		V
	3.3-V high-level CMOS output voltage	I_{OH} = –0.1 mA DC, V_{CCIO} = 3.0 V *(9)*	V_{CCIO} – 0.2		V
V_{OL}	5.0-V low-level TTL output voltage	I_{OL} = 12 mA DC, V_{CCIO} = 4.75 V *(10)*		0.45	V
	3.3-V low-level TTL output voltage	I_{OL} = 12 mA DC, V_{CCIO} = 3.00 V *(10)*		0.45	V
	3.3-V low-level CMOS output voltage	I_{OL} = 0.1 mA DC, V_{CCIO} = 3.0 V *(10)*		0.2	V
I_I	Leakage current of dedicated input pins	V_I = V_{CC} or ground	–10	10	µA
I_{OZ}	I/O pin tri-state output off-state current	V_O = V_{CC} or ground *(11)*	–40	40	µA

Altera M7000 Output Drive Current



Altera M7000 AC Op. Conds.

Table 13. MAX 7000 5.0-V Device Capacitance: EPM7032, EPM7064 & EPM7096 Devices *Note (12)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		12	pF
$C_{I/O}$	I/O pin capacitance	V_{OUT} = 0 V, f = 1.0 MHz		12	pF

Table 14. MAX 7000 5.0-V Device Capacitance: MAX 7000E Devices *Note (12)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Input pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		15	pF
$C_{I/O}$	I/O pin capacitance	V_{OUT} = 0 V, f = 1.0 MHz		15	pF

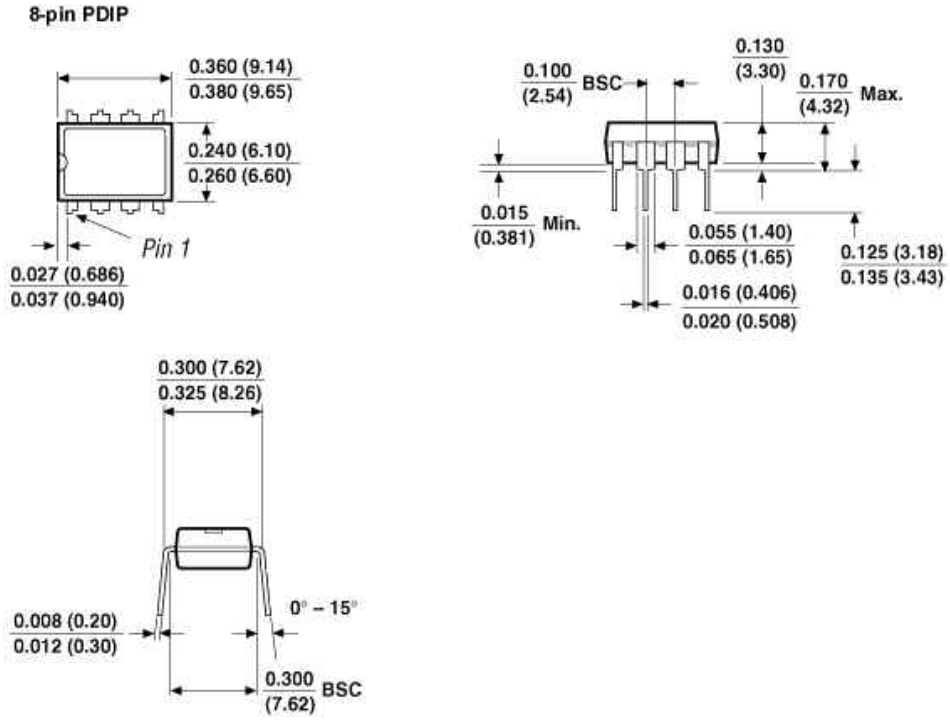
Table 15. MAX 7000 5.0-V Device Capacitance: MAX 7000S Devices *Note (12)*

Symbol	Parameter	Conditions	Min	Max	Unit
C_{IN}	Dedicated input pin capacitance	V_{IN} = 0 V, f = 1.0 MHz		10	pF
$C_{I/O}$	I/O pin capacitance	V_{OUT} = 0 V, f = 1.0 MHz		10	pF

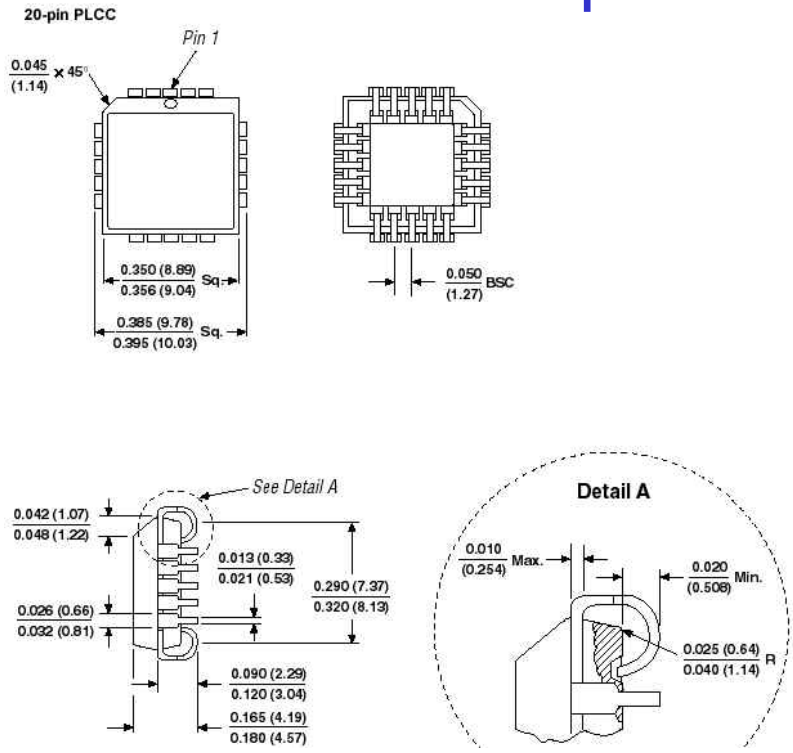
Packaging

- (P)(C)DIP – (Plastic/Ceramic) Dual In-Line
- PLCC – Plastic Leaded Chip-carrier
- SOIC – Small Outline Integrated Circuit
- PQFP – Plastic Quad Flat-pack
- PGA – Pin Grid Array (flip-chip)
- BGA – Ball Grid Array (flip-chip)

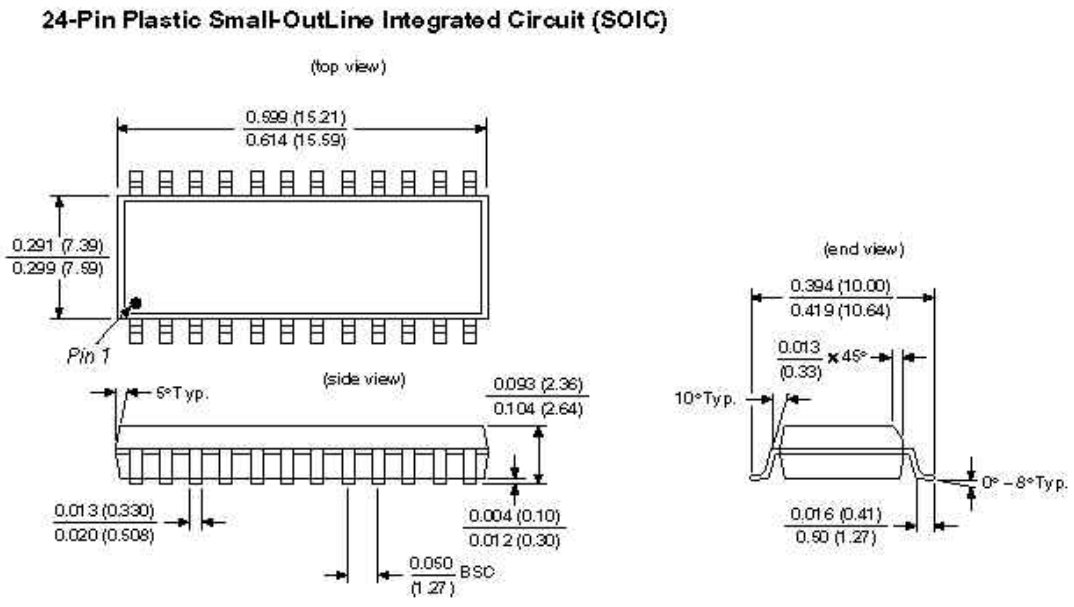
Plastic Dual In-line



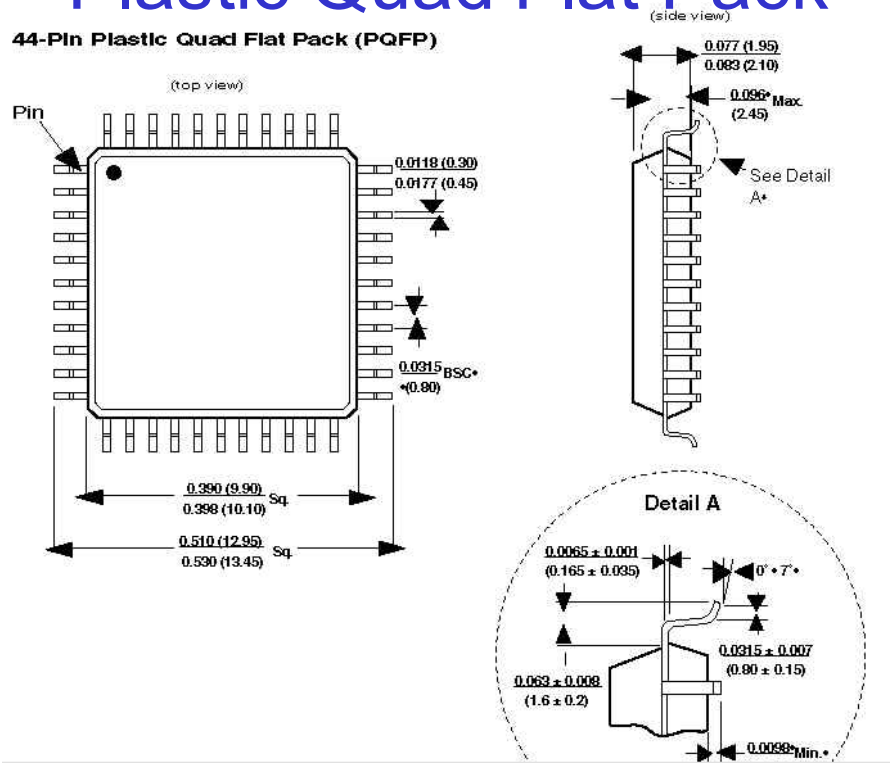
Plastic Leaded Chip-carrier



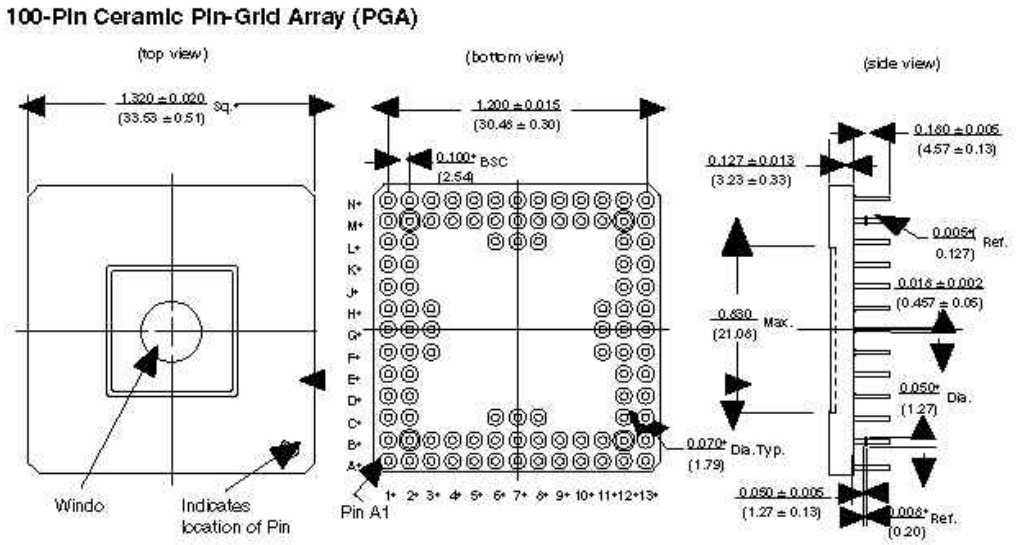
Small Outline Integrated Circuit



Plastic Quad Flat Pack



Ceramic Pin Grid Array



Ball Grid Array

49-Ultra FineLine BGA