Issues in FPGA Technologies

• Complexity of Logic Element
  – How many inputs/outputs for the logic element?
  – Does the basic logic element contain a FF? What type?

• Interconnect
  – How fast is it? Does it offer ‘high speed’ paths that cross the chip? How many of these?
  – Can I have on-chip tri-state busses?
  – How routable is the design? If 95% of the logic elements are used, can I route the design?
    • More routing means more routability, but less room for logic elements and can increase delay due to interconnect

Issues in FPGA Technologies (cont)

• Macro elements
  – Are there SRAM blocks? Is the SRAM dual ported?
  – Is there fast adder support (i.e. fast carry chains?)
  – Is there fast logic support (i.e. cascade chains)
  – What other types of macro blocks are available (fast decoders? register files? advanced IP cores? )

• Clock support
  – How many global clocks can I have?
  – Are there any on-chip Phase Locked Loops (PLLs) or Delay Locked Loops (DLLs) for clock synchronization, clock multiplication?
Issues in FPGA Technologies (cont)

• What type of IO support do I have?
  – TTL, CMOS, etc
  – Support for mixed 5V, 3.3V IOs?
    • 3.3V internal, but 5V tolerant inputs?
  – Support for other low voltage signaling standards?
    • GTL+, GTL (Gunning Transceiver Logic) – as used on Pentium II
    • HSTL - High Speed Transceiver Logic
    • SSTL - Stub Series-Terminate Logic
    • USB - IO used for Universal Serial Bus (differential signaling)
    • AGP - IO used for Advanced Graphics Port
  – Maximum number of IO? Package types?
    • Ball Grid Array (BGA) for high density IO

CPLDs and FPGAs

<table>
<thead>
<tr>
<th>CPLD</th>
<th>FPGA</th>
</tr>
</thead>
<tbody>
<tr>
<td>Complex Programmable Logic Device</td>
<td>Field-Programmable Gate Array</td>
</tr>
<tr>
<td>Architecture</td>
<td>PAL-like</td>
</tr>
<tr>
<td>Density</td>
<td>Low-to-medium</td>
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<tr>
<td>Up to 16 22V10s</td>
<td>1K to 125K logic gates</td>
</tr>
<tr>
<td>Performance</td>
<td>Predictable timing</td>
</tr>
<tr>
<td>Over 100 MHz</td>
<td>High-performance</td>
</tr>
<tr>
<td>Interconnect</td>
<td>“Crossbar”</td>
</tr>
</tbody>
</table>

**NOTE:** First generation programmable devices (PROMs, PALS, PLAs, GPLAs) Analogous to 2-level Logic while CPLDs/FPGAs (programmable interconnects) Analogous to Multi-level Logic
Programmable Logic Resources

1) Configurable Logic Blocks (CLBs) or Logic Elements (LEs)
   - Memory lookup tables
   - AND-OR planes
   - Simple gates

2) Input / Output Blocks (IOBs)
   - Bidirectional
   - Latches, inverters, pullup/down

3) Interconnect or Routing
   - Local and global routing balance
   - Delay and area

*Each of these three Basic Resources Require a Programmable Circuit*

Programming Technologies

1) Bipolar fusible link (not commonly used in modern devices)
   - Closed device, burned open by high current
   - Smallest Area-more complicated to fabricate
   - One Time Programmable (OTP)

2) Antifuse
   - Open device, closes with high voltage
   - Small area but high voltage required
   - One Time Programmable (OTP)

3) SRAM based
   - Uses pass transistor controlled SRAM cell
   - Large Area
   - Volatile (Reprogrammable)

4) E/EEPROM/Flash based
   - Moderate Area
   - Non-Volatile (Reprogrammed)
Metal to Metal Antifuse Technology

Unprogrammed Antifuse

Antifuse

Metal 3

Via to Metal 4

Programmed Antifuse

23-MAR-01

AMER 7.0 kV X80.6K 375nm
**Antifuse Technology**

Actel Programmable Low Impedance Circuit Element (PLICE)

- ONO (oxide nitride oxide) Dielectric insulates diffusion and poly
- ONO “melted” by applying 16V pulse across it

*Sources Hauck (IEEE Proc.), Actel Data Sheets 1994*

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**ONO Antifuse Technology**

(unprogrammed)

ONO Antifuse Photomicrograph
ONO Antifuse Technology
(programmed)

- Floating Gate (FG) is Completely Isolated
- Unprogrammed Transistor has no Charge on FG Operates Normal NMOS Transistor using Access Gate (AG) as gate
- Programmed by High Voltage on AG and Low Voltage on Drain Causing Neg. Charge on Floating Gate
- Source to Drain Path cannot be closed when programmed
- EPROM uses UV light to Discharge FG and erase
- EEPROM uses high voltages similar to programming but opposite polarity to erase

*Source Hauck (IEEE Proc.)
Pass Transistor is “on” during Programming and “off” during Normal Operation of Programmed FPGA

- Inverter Pair Latches Logic Value using the Upper “weak” Keeper Inverter
- Larger Area than E/EEPROM Based Cell
- More Easily Reprogrammed – Useful for Reconfiguration and Prototyping
- “Read” Function used for Debugging to Output Programmed Configuration

*Source Hauck (IEEE Proc.), Xilinx 1994, Compton

Q or Q’ Output from 1-bit SRAM Cell

- NMOS Pass Transistor

Routing Resource #1

Routing Resource #2

*Source Hauck (IEEE Proc.), Xilinx 1994, Compton
LE/CLB Structures

- Different Styles of Internal Structure
  - Look-Up Tables (LUTs)
  - PLA/PAL-based Macrocells
  - Arrays of Multiplexers
- Granularity Variations
- Delay Characteristics
- Internal Programming Technology
- Scalability - Logic Clusters

**Generic Look-Up Table (LUT)**

*Source Compton*
Registered/By-Pass Programmable Circuit

BYPASS bit is Programmed

*Source Compton

Generic LUT-Based LE

*Source Compton
Xilinx 6200 Logic Element

- Can Compute any 2-input and some 3-input functions
- Extremely Fine-grained
- Based on Multiplexers

*Source Compton

Increasing Granularity

\[ \text{OUT} = (\overline{A}BCD + ABCD + \overline{A}BC \overline{C})EF \]
\[ + (AB\overline{G} + A\overline{B}H)F \]

*Source Compton
Xilinx 4000 Series CLB

- 3 function generators
- CLB inputs
  - F1-F4 to F
  - G1-G4 to G
  - H1 (F & G) to H
- 4 CLB outputs
  - F, G, or H
  - and registered

More Detail on Next Slide

Figure 1: Simplified Block Diagram of XC4000 Series CLB (RAM and Carry Logic functions not shown)
Device Architectures

- Proportion of Interconnect Resources Versus Logic Elements
- Routability Among Logic Elements
- Dedicated Interconnections Among Logic Elements
- Granularity
- Hierarchical versus Flat Interconnections

Routing Architectures

- Symmetrical
- Row Based
- Sea of Gates
- Routing Matrix
Conceptual Diagram of Island-style Architecture

Xilinx 4000 Series Architecture
Actel-like Row-based Architecture

Altera Flex10k Architecture

Figure 1. FLEX 10K Device Block Diagram
Altera Flex10k Architecture

• Hierarchical Interconnection Among Logic Elements
• Logic Arrays consist of 8 Logic Elements
• Each Embedded Array Block (EAB) has 2K bits of storage
• Architecturally in center of device
• LA and EAB connect to surrounding channel interconnect
Interconnect Structures

- Programmable Interconnects Generally Dominant Factor in Area and Delay
- Composed of Drivers on Wires and Switch Blocks
- Bidirectional Allow Signal Flow in Either Direction
- Directional Allow Signal Flow in One Direction Only
- Routing Accomplished via Switch Block and Driver Programming Bits
Bidirectional and Directional Interconnects

Interconnect Switch Blocks

Horizontal and Vertical Crossings Represent Programmable Switch Blocks

*Lemieux et al., ICFPT 2004*
Bidirectional Switch Block

Programmable Single-bit Cells
*Lemieux et al., ICFPT 2004

Directional and Bidirectional Switch Blocks

*Lemieux et al., ICFPT 2004
Commercial Trends Circa-2000

• Three main types: Antifuse, Flash, SRAM

Alterna FPGA Family Examples

• Altera Flex10K/10KE
  – LEs (Logic elements) have 4-input LUTS (look-up tables) +1 FF
  – Fast Carry Chain between LE’s, Cascade chain for logic operations
  – Large blocks of SRAM available as well

• Altera Max7000/Max7000A
  – EEPROM based, very fast (Tpd = 7.5 ns)
  – Basically a PLD architecture with programmable interconnect. (CPLD)
  – Max 7000A family is 3.3 v
Xilinx FPGA Family Examples

• Virtex Family
  – SRAM Based
  – Largest device has 1M gates
  – Configurable Logic Blocks (CLBs) have two 4-input LUTS, 2 DFFs
  – Four onboard Delay Locked Loops (DLLs) for clock synchronization
  – Dedicated RAM blocks (LUTs can also function as RAM).
  – Fast Carry Logic

• XC4000 Family
  – Previous version of Virtex
  – No DLLs, No dedicated RAM blocks

Actel FPGA Family Examples

• MXDS Family
  – Fine grain Logic Elements that contain Mux logic + DFF
  – Embedded Dual Port SRAM
  – One Time Programmable (OTP) - means that no configuration loading on powerup, no external serial ROM
  – AntiFuse technology for programming (AntiFuse means that you program the fuse to make the connection).
  – Fast (Tpd = 7.5 ns)
  – Low density compared to Altera, Xilinx - maximum number of gates is 36,000
Cypress CPLD Example

• Ultra37000 Family
  – 32 to 512 Macrocells
  – Fast (Tpd 5 to 10ns depending on number of macrocells)
  – Very good routing resources for a CPLD

SPEED Trends

FPGA Performance: 25% Growth Rate
2000: 100+ MHz - 1,000,000 Equivalent Logic Gates
1998: 60-80 MHz - 250,000 Equivalent Logic Gates
Delay Trends (‘95)

Effects of Scaling of Interconnection

![Graph showing Delay Trends for Interconnect Delay (RC) and Intrinsic Gate Delay as a function of feature size.](image)

Comparison of intrinsic gate delay and interconnect delay (RC) as a function of feature size. In sub-micron technologies, the interconnects delay becomes the dominant factor. Marzola 1995

Density Improvements

![Graph showing FPGA Density Projection: 50% to 60% Annual Growth Rate.](image)

FPGA Density Projection: 50% to 60% Annual Growth Rate
1998: 250,000 – 2000: 1,000,000 Equivalent Logic Gates
Summary

- Different FPGA/CPLD Device Technologies Offer Varying Performance/Area and Other Attribute Tradeoffs
- PLDs Less Flexible than FPGA/CPLD since no Programmable Interconnect Feature
- Reprogrammability
- Security
- Volatility
- Power Consumption
- Power-up Configuration
- Radiation Tolerance