EE 2381 Digital Computer Logic

Introduction and Overview:
– Analysis and Design
– Combinational and Sequential Circuits
– Simulation vs Hardware

EE 2381 Digital Logic Lecture

• Digital computers and information; combinational logic circuits; combinational logic design; sequential circuits including finite-state machines; registers and counters; memory and programmed logic design.
• Design and simulation of digital computer logic circuits are studied.
EE 2181 Digital Logic Laboratory

- Analysis and synthesis of combinational and sequential digital circuits.
- Basic digital logic circuits are designed, simulated using Verilog HDL and implemented using a Digi-Designer kit and integrated circuits.

Goal: Analysis and synthesis of combinational network:

\[ f(A, B, C) = AB + (BC)' \]
**Goal:** Analysis and synthesis of sequential network

\[
f(A, B, C) = AB + (BC)'\]

```verilog
module MAIN;                       // Combinational Network Simulation
    reg A, B, C;
    wire D, E, F;

    and #(17,12) u01A(D, A, B);     // AND gates
    nand #(11,07) u02A(E, B, C);     // NAND gate
    or   #(10,14) u03A(F, D, E);     // OR gate

initial
    begin
        $monitor($time," - A=%b B=%b C=%b D=%b E=%b F=%b",A,B,C,D,E,F);
        #100 A=0;B=0;C=0;
        #100 A=0;B=0;C=1;
        #100 A=0;B=1;C=0;
        #100 A=0;B=1;C=1;
        #100 A=1;B=0;C=0;
        #100 A=1;B=0;C=1;
        #100 A=1;B=1;C=0;
        #100 A=1;B=1;C=1;
        #100 $finish;
    end
endmodule
```