Review Mano & Ciletti Text: Chapter 3, section 9 and Chapter 5, sections 1-4 and 8 (focus on excitation tables and maps for flip-flop inputs).

1. The adder-subtractor circuit shown in Fig 4-13 on page 142 has the following values for the mode input $M$ and data inputs $A$ and $B$. In each case, determine the values of the four SUM outputs, the carry $C$, and overflow $V$.

$$
\begin{array}{c|c|c|c|c|c|c}
M & A & B & C & V \\
\hline
(a) & 0 & 1001 & 0101 & & \\
(b) & 0 & 0101 & 1101 & & \\
(c) & 1 & 1101 & 1100 & & \\
(d) & 1 & 0010 & 0110 & & \\
\end{array}
$$

2. Mano & Ciletti 5-1. Use Verilog to verify your circuits operation.

3. Assume the following operations and values for a flip-flop with the inputs $P$ and $N$:

<table>
<thead>
<tr>
<th>Operation</th>
<th>PN</th>
</tr>
</thead>
<tbody>
<tr>
<td>No Change</td>
<td>10</td>
</tr>
<tr>
<td>Clear to 0</td>
<td>00</td>
</tr>
<tr>
<td>Set to 1</td>
<td>11</td>
</tr>
<tr>
<td>Complement</td>
<td>01</td>
</tr>
</tbody>
</table>

a. Tabulate the characteristic table
b. Derive the characteristic equation
c. Tabulate the excitation table
d. Show how this flip-flop can be converted to a $D$ flip-flop.

4. Design a counter which counts in the following sequence: 000, 011, 101, 100, 111, 000, … using positive edge-triggered $D$ flip-flops and NAND gates.