Multiple-Valued Logic Memory System Design Using Nanoscale Electrochemical Cells

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Abstract

Nanoscale multiple-valued logic systems require the development of nanometer scale integrated circuits and components. Due to limits in device physics, new components must be developed to operate at the nanoscale level. As part of this effort, the authors have constructed nanoscale electrochemical cell arrays that can function as multiple-valued logic storage cells. In addition, the authors are currently developing a nanoscale crossbar system that will use these cells to implement multiple-valued logic memory units. This paper describes the development of these cells and their applications.

1. Introduction

Traditional computer systems use binary logic for their operations. However, using multiple-valued logic, or MVL, can help improve the efficiency of arithmetic operations. For example, a ternary number (base 3) can be represented by {-1, 0, 1}. This allows for balanced number representations as opposed to the binary number system. The balance allows for redundancy, which enables fast arithmetic operations [1]. Multiple-valued logic circuits can also reduce the number of operations required to implement particular mathematical functions. This will result in chips with reduced area and power dissipation [2].

The transition from microscale to nanoscale circuits will require a new approach to chip design. Traditionally, CMOSFET's have been scaled by simultaneous reduction of device dimensions and supply voltages. However, this scaling will eventually reach physical limits as it reaches the nanometer range. Therefore, new devices will need to be developed that address these limits [3]

Microscale computer system designs often use "course-grained" architectures such as multiple processor blocks. This approach is used because of the high overheads imposed by reconfiguration techniques in devices such as FPGA's. However, nanoscale computer systems will likely be formed from arrays of simple cells with highly localized interconnections. This will occur since nanodevices will likely evolve towards molecular and/or quantum/single electron technologies. Using MVL may result in the reduction of overhead to allow use of "fine-grained" nanoscale devices [4]. An important part of this effort will be the development of MVL nanoscale memory systems that can store the ternary (base 3) or quaternary (base 4) numbers that will be used by MVL arithmetic circuits.

Most of the recent developments on nanoscale MVL memory designs focus on hybrid devices, such as combining CMOS with SET (Single-Electron Transistors) [5, 6]. The authors are exploring a new approach to memory that may be applicable to multi-valued logic value storage at the nanoscale level: the use of nanoscale electrochemical cells that may be charged and discharged to different levels. The approach is based on the authors' previous application for traditional binary memory cells [7]. This paper describes the design of the storage cells and their implementation as memory circuits.

2. Nanoscale electrochemical cells

The concept of nanoscale electrochemical cells for memory is based on previous work by Teeters in the area of nanobattery development and characterization. This work has been concerned with the construction of individual nanometer scale battery arrays containing nanometer scale components, including nanoscale cathodes and anodes and their characterization [8-14]. Teeters' group developed the methods to make arrays of these cells using commercially available nanoporous alumina membranes (Synkera Technologies, Longmont, CO) having hexagonally ordered pores. These pores can range from several hundred nanometers to smaller than 10 nanometers in diameter. The thickness of the membranes is a maximum of 60

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microns or less. The techniques for making nanobattery arrays have been developed by Teeters' group [8, 13, 14] and will be summarized below.

Arrays of nanocells are made by sealing one side of the membrane with a polymer film and applying a coating of sol-gel electrolyte material such as V_2O_5 on the opposite side. Since the nanopores in the membrane are sealed on one side, the sol-gel can only partially penetrate into the pores. The sol-gel is then cured forming the electrodes for this side of the membrane. Excess sol-gel that is above the membrane pores has been found to simply slough off leaving individual nanoscale electrodes for the arrays of nanocells at the surface. The polymer seal is then removed from the other side of the membrane by use of a solvent opening the nanopores on this side. A molten poly(ethylene oxide) polymer/inorganic salt electrolyte is introduced into the open pores facilitated by capillary action under vacuum conditions. This side of the membrane is then placed on a continuous layer of electrode material. This is illustrated in Figure 1.

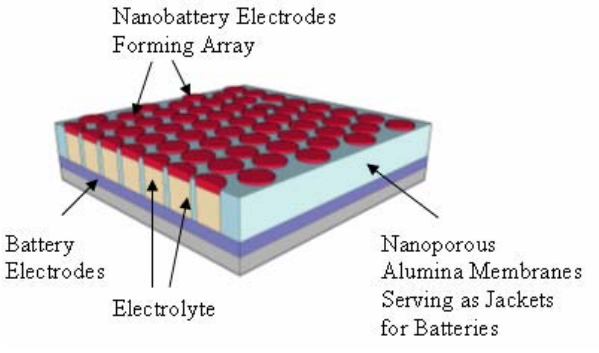

Figure 1. Nanoscale electrochemical storage cells.

Storage of multiple-valued logic data

To date, nanoscale cathodes and anodes have been coupled with a polymeric electrolyte confined in pores in nanoporous alumina membranes, 200 nm and smaller, to make individual cells having nm sized electrodes. At present, the nanoscale electronic circuits that can be fabricated are limited in terms of available nanoscale circuit components and interconnection methods. Teeters' group developed the advanced techniques necessary to conduct tests on individual micro and nanocells, such as charge/discharge studies, a.c. impedance spectroscopy and other electrochemical tests [8- 10, 12-14] by using the cantilever tip of an electrically conducting tip of an atomic force microscope (AFM) to make contact with the nanoelectrodes. If this tip conducts electrically, it can be touched to the small cathode or anode particle, making electrical contact so that the battery can be charged and tested.

Figure 2 shows charge/discharge data collected by using the tip of an AFM cantilever to make electrical contact with the 200 nm in diameter anode of the nanocell. A charge current of 60 picoamps of current was used while 5 picoamps was used as the discharge current. At this rate of charge it takes approximately 100 seconds to reach its full charge of 3.5 volts. At this discharge rate of 5 picoamps, approximately 10 minutes are required to totally discharge the individual nanocell.

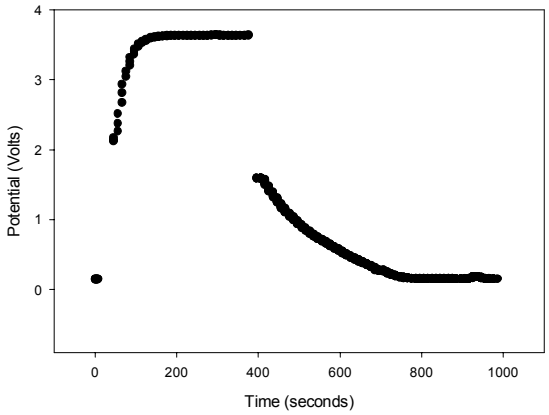

Figure 2. Charge/discharge data for an individual nanocell.

For binary memory applications, a charged cell represents a "1" value, while a discharged cell represents a "0" value. The high and low voltage values depend on the supply voltage and noise margins for a given logic circuit. However, for MVL memory applications, the system radix (base) will also need to be considered. For example, a quaternary (base 4) system will need to define the voltage levels and noise margins for levels "0", "1", "2", and "3". In this case, the nanocell will be charged to the appropriate level to represent one of these values. As noted above, the nanocell charging and discharging times depend on the cell current and voltage swing. For multiple valued logic applications, the voltage thresholds would need to be selected to minimize switching time. Therefore, possible voltages thresholds for a quaternary system may be 0, 0.25, 0.5, and 0.75 volts for the respective logic levels.

3. Memory array design

A nanoscale MVL memory system will require an array of these nanocells, which will be placed on a

continuous electrically conducting substrate. If a nanobattery is later touched by a tip, seeking information, the tip will sense a voltage or current because the nanobattery has been charged (higher voltage or current). If this particular battery had not been charged, the tip will sense no voltage or current. In this manner, data can be "saved" and "read" from the nanobattery memory array. Because such small amounts of current would be used during the reading process, these cells could in effect function as nonvolatile memory. Recording and retrieving data using the tip of an atomic force microscope would provide the necessary means to develop and characterize these nanobattery arrays. However, reading data at a rate fast enough for practical memory application would simply not be possible. A system under development by IBM called the Millipede system [15, 16] gives nanobattery arrays the potential to have technological utilization. IBM's system consists of arrays of AFM cantilevers. Thus far, they have used arrays of cantilevers that are 64 x 64. A nanobattery array could be accessed for their stored information in a similar manner. However, an array of cantilever AFM tips could be used to access the array of nanocells at an acceptable rate [15-17]. In this process, one tip would access numerous nanobattery memory elements. Because there are now many tips accessing the array of nanocells, the speed of data acquisition is greatly increased. A specific cantilever tip is accessed by the grid of electrical contacts on the cantilevers. This system still has its limitations. The construction of a functioning large array of cantilevers is difficult and its operation can be cumbersome. Therefore, we are exploring an alternate approach to interconnect these nanocells, which is the use of crossbar circuits.

Nanocrossbar circuits for multiple-valued memory units

A successful nanoelectronic structure that can access arrays of elements is the crossbar circuit (Figure 3), where the memory array is formed from sets of parallel nanowires crossing each other at right angles, with a memory storage cell at each intersection [18]. A demultiplexer (demux) is used to select the column and row of the desired memory cell location.

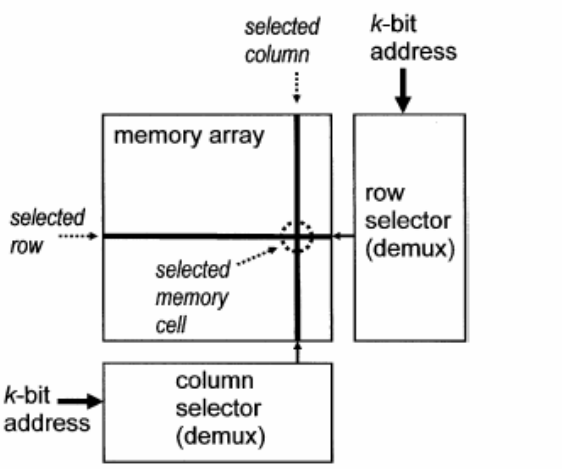

Figure 3. Nanoscale memory array using crossbar structure [18].

There are several advantages to using the crossbar circuit structure for nanoscale memory units. First, wire dimensions can be scaled down to molecular sizes, while the number of wires in the memory array can be scaled up to accommodate additional memory storage cells. Next, only 2k address wires are required to individually address 2^{2k} memory cells using the demultiplexers; this feature also helps to accommodate additional memory storage. Finally, the crossbar structure has been shown to be feasible and potentially inexpensive to fabricate at the nanoscale level [19].

Each memory cell in the crossbar array must be able to store a logic value, and allow this value to change as directed by the crossbar selection wires. While switching can represent a logic state, it also is important for a memory cell to be able to store the value of the logic state for extended periods of time. Therefore, the authors are investigating the use of nanoelectrochemical cells for this purpose, where a cell is charged to a voltage that represents the desired logic level. The wires on each side would be at angles to each other such that a nanobattery would be between the crossing nanowires thus forming the crossbar system. This is illustrated in Figure 4 where the alumina membrane has been removed from the figure so the nanobattery crossbar system can be better seen. Not only will this system work for the basic design of nanoscale storage units, but also ordered arrays of battery electrodes of this size would result in memory systems of expanded capacity. Based upon calculations completed by IBM researchers, information stored with this density would be able to exceed the limit predicted for magnetic data storage systems [15-17].

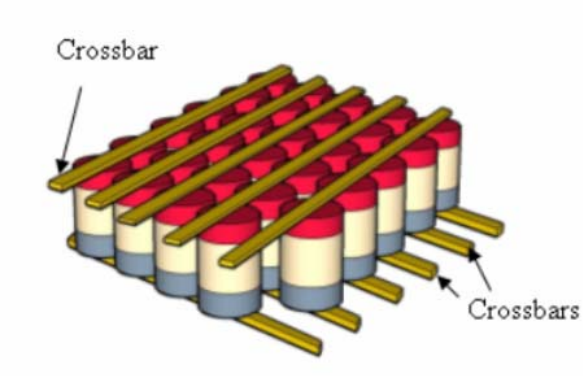

Figure 4. Nanoscale memory unit design using nanocells with crossbar arrays.

For multiple logic value memory circuits, the crossbar decoders will need to be able to handle multiple level logic addressing. The approach described in [20] has potential applications for the proposed nanocell crossbar array.

4. Conclusion and future work

Nanoscale memory systems require the development of nanoscale devices to implement the various system units. The authors have developed a nanoscale electrochemical to store MVL values, and are currently developing crossbar systems to interconnect these cells to implement nanoscale MVL memory systems. It is anticipated that the successful implementation of this technology will result in high-density memory systems that will be capable of storing data for various multiple-valued logic applications.

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