Partitioning Effects on Estimated Wire Length for Mixed Macro and Standard Cell Placement

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1.   Introduction

The integration of logic synthesis and physical design stages will become more important to meet the challenges of integrated circuit design as device densities continue to grow and feature sizes continue to shrink [1, 2]. Many contemporary designs use a combination of macro cells and standard cells to implement the desired system functions. In a typical design, there are usually many more standard cells than macro cells. Therefore, after the netlist has been formed by the logic synthesis stage, the standard cells are partitioned into groups, or *domains*, in order to reduce the total number of components to be initially placed during the physical design stage.

Because netlists can be modeled by a hypergraph [3], domains are created by applying hypergraph partitioning [4]. The criteria for hypergraph partitioning are to minimize the number of edges between partitions and to have groups of equal sizes (same number of vertices). There appears to be no criteria for number of domains, thus this quantity is often arbitrarily selected. However, the resultant grouping of the standard cells may not be the best arrangement for a given design.   Our previous work explored the relationship between the number of domains and placement performance: we found that increasing the number of domains also increased the time required to converge to an optimal layout [5].   The next area of research is to study the effects of partitioning decisions on solution quality.

An important objective for integrated circuit design is to meet the specified system timing requirements. For physical design, this requires that the cells are placed and routed such that the signal propagation delays through the circuit are minimal. Kapadia [6] uses partitioning in an attempt to meet timing requirements for standard cell layout. His method requires detailed information about gate load capacitances; these are composed of junction and diffusion capacitances of the transistors that form the gate [7]. However, the reduction in transistor sizes for standard cell circuits implies that interconnection wire delays will become more significant than gate delays [2]. The dominant factor for interconnection wire delay is wire length: longer wires increase signal propagation delays. During the placement stage, interconnection wire lengths are estimated based on the arrangement of components and net connections. This paper describes a statistical analysis to determine the effects of standard cell partitioning on estimated wire lengths.

2.   Method

The mixed macro and standard cell netlist from the MCNC benchmark suite were used in our experiments [8]. Table 1 shows the specifications for these netlists. Recall that one of the objectives of hypergraph partitioning is to divide a given set into equally-sized subsets. If we divide the standard cells of each netlist into 10, 20, 30, 40, and 50 domains, then we get the number of standard cells per domain as shown in Table 2. Based on these data, we determined that netlist g2 was too small to yield meaningful information. Thus, we selected netlists a3 and t1 for our study.

The hMetis multilevel hypergraph partitioning tool [4] was selected to create domains, while the GAP mixed macro and standard cell placement tool [9] was selected to perform the layout for the resultant netlist partitioning. Interconnection wire lengths are estimated using the *half-perimeter wire length* metric [10]. For each net, the total wire length is estimated by constructing a bounding rectangle that encloses all component terminals that connect to the net. Then, the half-perimeter wire length of the net is the sum of the length and the width of the bounding box, or $\Delta x + \Delta y$ as shown in Figure 1.

GAP uses a genetic algorithm to optimize placement. Genetic algorithms are *stochastic*: there are a number of random events that occur during the algorithm operation. Therefore, for a given input, separate runs of the genetic

algorithm will produce different outputs for the same input parameters. This implies that one run of GAP for each partitioning result would not produce sufficient data for analysis. Thus, ten trials were run for each group, and statistical tests were applied to analyze each data set.

3. Experimental results

The hMetis partitioning tool created 10, 20, 30, 40, and 50 domains for each netlist a3 and t1. GAP was run ten times for each data set to produce wire length results. The SAS® program was used to perform statistical tests on the data [11, 12].

First, we needed to determine if variations in the number of domains affected the performance of the placement tool. ANOVA (*ANalysis Of VAriance*) [13] was applied to the data. During the ANOVA procedure, an *F test* is performed which produces a *P-value*. If the P-value is less than or equal to the selected *level of significance* α, then the null hypothesis H_0 is rejected. This indicates that there is strong evidence that a significant relation exists between the dependent variable and independent variable. Otherwise, if the P-value is greater than α, then a significant relation cannot be identified. For our tests, we selected the default value $\alpha = 0.05$. The resultant P-values for wire lengths of netlists a3 and t1 were both 0.0001, thus there was strong evidence that estimated wire lengths are affected by variances in the number of domains.

ANOVA can identify if there are significant differences between at least two means. However, when comparing more than two means, ANOVA does not identify the specific means that are significantly different. For each netlist, we have five means: these are the mean wire length results for ten runs on each domain set (10, 20, 30, 40, 50 domains). In order to obtain more detailed information about the differences among the means, multiple comparison tests must be run. We used Duncan's Multiple Range Test [14] to determine if the differences between all sets of means were statistically significant. Table 3 shows the results of Duncan's test – these include the estimated mean wire lengths for each netlist and number of domains. All differences between the means were found to be statistically significant for $\alpha = 0.05$.

4. Discussion

Figure 2 shows how the mean estimated wire lengths vary with number of domains for netlist a3 and t1. Note that there is a direct relationship between number of domains and mean estimated wire lengths. Recall Table 2 - as we increase the number of domains, we reduce the number of standard cells per domain. For a given netlist,

there may be standard cells that share a large number of common interconnections - these cells are *strongly-connected*. If we increase the number of domains, it is likely that we will split apart groups of strongly-connected cells during the partitioning process, thus wire lengths of the common nets will increase. This assumption has been verified by our statistical results.

Our long-term goal is to find an algorithm that estimates the best partition size with respect to layout results. This will require an examination of other partitioning methods and connectivity models, and finding a representation sample of circuits to get meaningful results.

5. References

[1] M. Breuer, M. Sarrafzadeh, and F. Somenzi, "Fundamental CAD Algorithms," *IEEE Trans. Comp.-Aided Design*, vol. 19, pp. 1449-1475, 2000.

[2] K. Keutzer, A. R. Newton, and N. Shenoy, "The Future of Logic Synthesis and Physical Design in Deep-Submicron Process Geometries," presented at the 1997 Int. Symp. Physical Design (ISPD '97).

[3] T. Cormen, C. Leiserson, and R. Rivest, *Introduction to Algorithms*: MIT Press, 1990.

[4] G. Karypis, R. Aggarwal, V. Kumar, and S. Shekhar, "Multilevel Hypergraph Partitioning: Application in VLSI Domain," presented at the 34th ACM/IEEE Design Automation Conf., 1997.

[5] T. W. Manikas and G. R. Kane, "Standard Cell Partition Size Variance and its Effect on Physical Design," presented at the10th IEEE/ACM Int. Workshop on Logic & Synthesis, 2001.

[6] H. Kapadia and M. Horowitz, "Using Partitioning to Help Convergence in the Standard-cell Design Automation Methodology," presented at the 36th ACM/IEEE Design Automation Conf., 1999.

[7] J. M. Rabaey, *Digital Integrated Circuits: A Design Perspective*: Prentice-Hall, 1996.

[8] CBL, "MCNC benchmark suite," Collaborative Benchmarking Laboratory, North Carolina State University.

[9] T. W. Manikas, "A Genetic Algorithm Approach for Mixed Macro and Standard Cell Placement that Directly Incorporates Cell Membership Information," Ph.D. thesis, Dept. of Electrical Engineering: University of Pittsburgh, 1999.

[10] D. G. Schweikert, "A 2-dimensional Placement Algorithm for the Layout of Electrical Circuits," presented at the 13th ACM/IEEE Design Automation Conf., 1976.

[11] *SAS Languages and Procedures*. Cary, NC: SAS Institute, Inc., 1990.

[12] R. P. Cody and J. K. Smith, *Applied Statistics and the SAS Programming Language*, 4th ed. Upper Saddle River, NJ: Prentice-Hall, 1997.

[13] J. Neter, W. Wasserman, and M. Kutner, *Applied Linear Statistical Models: Regression, Analysis of Variance, and Experimental Design*, 3rd ed. Burr Ridge, IL: Irwin, 1990.

[14] B. J. Winer, D. R. Brown, and K. M. Michels, *Statistical Principles in Experimental Design*, 3rd ed: McGraw-Hill, 1991.

Table 1. Benchmark netlist data.

Netlist	Macro Cells	Standard Cells	Nets
a3	25	519	933
g2	17	113	377
t1	26	432	1138

Table 2. Standard cells per domain.

Number of Domains	a3	g2	t1
10	51.9	11.3	43.2
20	26.0	5.7	21.6
30	17.3	3.8	14.4
40	13.0	2.8	10.8
50	10.4	2.3	8.6

Table 3. Results of Duncan's test – mean estimated wire lengths.

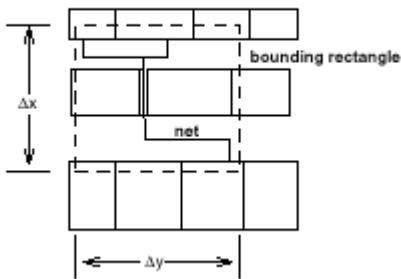| Netlist	# of domains				
a3	10	20	30	40	50
mean	1697259	1861669	2012529	2199831	2343594
t1	10	20	30	40	50
mean	2876535	3067082	3392072	3601277	3795495

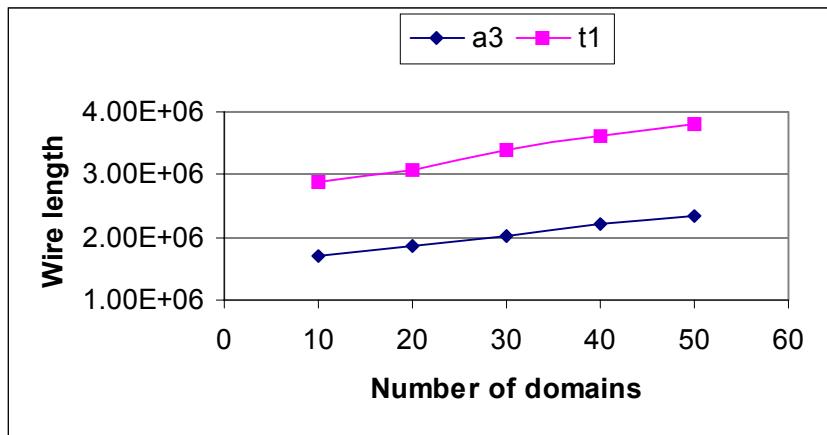**Figure 1. Half-perimeter wire length of a net.**

Figure 2. Mean estimated wire lengths vs. number of domains.