Low Power Shift and Capture through ATPG-Configured Embedded Enable Capture Bits

Yi Sun*, Hui Jiang*, Lakshmi Ramakrishnan*, Jennifer Dworak*,
Kundan Nepal†, Theodore Manikas*, and R. Iris Bahar‡
* Lyle School of Engineering, Southern Methodist University, Dallas Texas, 75205
†School of Engineering, University of St. Thomas, Saint Paul, Minnesota 55105
‡School of Engineering and Department of Computer Science, Brown University, Providence, Rhode Island 02912

2021 IEEE International Test Conference (ITC) | 978-1-6654-1695-5/21/$31.00 ©2021 IEEE | DOI: 10.1109/ITC50571.2021.00045

***Abstract*—Excessive test power can cause multiple issues at manufacturing as well as during field test. To reduce both shift and capture power during test, we propose a DFT-based approach where we split the scan chains into segments and use extra control bits *inserted between the segments* to determine whether a particular segment will capture. A significant advantage of this approach is that a standard ATPG tool is capable of automatically generating the appropriate values for the control bits in the test patterns. This is true not only for stuck-at fault test sets, but for Launch-off-Capture (LOC) transition tests as well. It eliminates the need for expensive post processing or modification of the ATPG tool. Up to 37% power reduction can be achieved for a stuck-at test set while up to 35% reduction can be achieved for a transition test set for the circuits studied.**

***Index Terms*—DFT, Low Power Test, On-Chip Decompressor, Stuck-At faults, Transition faults**

I. Introduction

Power during scan based test is usually much higher than the power expended in functional mode [1]. Excess power during test can cause IR drop, increase circuit delays, cause integrated circuits (ICs) to have hot spots, and in some cases even damage or reduce the life expectancy of a chip. In field test, parts may also be exposed to high temperature environments due to weather or other heat-producing components in other parts of the system. Thus, effective techniques to reduce the power per pattern and reduce the total power expended during test are needed [1].

A significant amount of low power test research has focused on shift power because most of the energy expended during test comes from scan shift. This is partially because many more testing clock cycles are devoted to shift than to capture. One of the simplest approaches to reducing shift power is "adjacent fill." In the adjacent fill approach [2] don't care bits in the test patterns are filled with the value of an adjacent care bit. This reduces the number of times the flip-flops toggle during shift while maintaining the fault coverage of the patterns.

Alternative approaches to reducing shift power have also been proposed. One technique involves staggering multiple clocks so that different regions will shift and/or capture data out of phase (e.g., [3]–[5]). Others have kept entire chains or groups of chains from shifting (e.g., [6]). These approaches can certainly reduce power, but they tend to do so at a coarse level of granularity—at the level of a chain, group of chains, or clock domain. Additional approaches may re-order scan cells to match a particular test pattern set or test pattern generation procedure.

Other researchers have investigated reducing power during capture [7]–[9]. As testing proceeds, only a few new fault detections occur with each pattern. While the flip-flops that capture the test results for those new detections must continue to capture, fault coverage can be maintained even when the *other* flip-flops do not capture. This is valuable because preventing a flip-flop from capturing not only reduces the switching activity arising from that flip-flop itself, but it also generally prevents switching in the combinational logic in that flip-flop's downstream cone-of-influence.

Unfortunately, the presence of an on-chip decompressor also increases the difficulty of reducing test power. When an on-chip decompressor is used, many of the othewise "don't care" bits in the scan chain may need to be filled to satisfy the needs of the on-chip decompressor algorithm. An ATPG tool may allow the on-chip decompressor patterns to be generated in low power mode, but the overall reduction that can be achieved must also satisfy the needs of the decompressor.

In this paper, we focus on reducing test power in both the shift and capture stages in the presence of an on-chip decompressor. To achieve this, we split scan chains into smaller scan segments whose ability to capture data during the capture cycle is dependent on each segment's EECB (Embedded Enable Capture Bit), which is placed *in the chain in between the segments.* Because of the way the circuitry is designed, the ATPG tool is able to *automatically generate appropriate values for the EECBs* to enable capture when the corresponding segment is needed for targeted fault detection by that test pattern. Ideally, at other times each EECB will be set by the ATPG tool to deny segment capture to reduce power draw (although this is not guaranteed). ***This new approach removes the need for the expensive post-processing required by our previous approach in addition to the potential need for additional scan pins. It also allows us to automatically target transition faults with a Launch-off-Capture (LOC) test set.*** We will show that with low area overhead reported from the synthesis tool, we can achieve effective power reduction across multiple circuits—even when compared with low-power patterns generated by an ATPG tool for traditional scan chains that do not contain deny-capture segments.

This work was supported by NSF CCF1812777 and CCF1814928.

978-1-6654-1695-5/21/$31.00 ©2021 IEEE
DOI 10.1109/ITC50571.2021.00045

Short Paper

II. Previous work

A number of test generation techniques and DFT architectures have previously been proposed to reduce test power during scan shift and/or capture. ATPG based techniques that focus on reducing shift include test-vector modification [10], test-vector reordering [11], and X-filling techniques such as adjacent fill [2], [12]. The work of [9], [13], [14] proposed methods to reduce shift power in the presence of an on-chip decompressor. For example, [13] modified the decompressor to allow a constant value of 0 to be shifted into a group of chains over multiple shift cycles, where XOR tree logic or a PRPG (Pseudo Random Pattern Generator) generates appropriate values for the control register. Related work in [9] noted that scan chains that only load constant values could be kept in shift mode when the test is applied to reduce the power of scan chain unload as well.

Different X-filling techniques (e.g. [7], [8]) that focus on reducing power by reducing switching during capture cycles have also been proposed. Reducing capture power by disabling one or more flip-flops (e.g. [15], [16]) or even scan chains (e.g. [6], [17]) have been proposed by a number of researchers. The authors of [15] proposed a technique to identify the propagation path of the faults and then reorder the flip-flops into chains so only flops that are detecting faults are capture-enabled. The authors of [16] proposed clock gating flip-flops to reduce capture power. The authors presented a process of adding DFT hooks to easily and selectively clock gate a flip-flop and then modified the test pattern generation procedure to take advantage of these additional hooks. In [6], the authors created a low-power BIST architecture that breaks the scan chains into groups that can be disabled together, allowing constant values to be supplied to sub-circuits of the combinational logic. In [17] multiple small scan chains are created by appropriately grouping the flip-flops, and clock gating is used to allow only one of the small chains to shift and/or capture data at a time. The grouping of the flip-flops was optimized to match don't care values in a particular test set. In [18] a "Capture in Turn" technique is proposed. In that paper, flip-flops are not grouped based upon a particular test set. A "cyclic shift register" is used to select chain i to shift data in while shifting out old test responses from chain i. Then the the cyclic shift register is advanced to select chain $i+1$, which captures data. Then new data can be shifted into chain $i+1$ while shifting out the captured test responses. The cyclic shift register advances again, and the process repeats.

Our approaches complement this previous work. In [19], we introduced an approach that divided the scan chain into multiple scan segments that could be enabled or disabled during each capture cycle. This approach was scalable and compatible with on-chip decrompressors. It also didn't require that the test set be known *a priori* to insert the required DFT logic. It could use whatever test set was generated by the ATPG tool without modification.

However, the approach presented in [19] also had some disadvantages. A separate control chain was used to control whether or not each of the segments would capture data during a particular test pattern. Because we used an existing ATPG software tool that was not modified, this required extensive post processing of fault simulation data to determine what values should be fed into the control chain. The control chain was also connected to an input that bypassed the on-chip decompressor.

In this paper, we explore an alternative approach that removes the need for the extensive post-processing by embedding the segment control bits within the chains themselves. *Because of the way the control is designed, a standard ATPG tool is capable of automatically producing the appropriate values of those control bits to achieve the desired fault coverage for both stuck-at and LOC transition patterns.* The values for the control bits can be set by shifting data into the normal functional chains in which the control bits are embedded. As a result, the approach is also compatible with an on-chip decompressor. Finally, when inserted into a full-scan design that already contains flip-flops with an enable input (such as for clock gating), no additional logic must be inserted in the paths of the functional logic—minimizing the impact on the functional circuit delay.

In the following sections, we demonstrate that our solution can achieve effective power reduction for multiple test patterns and for a variety of circuits.

III. Proposed DFT Architecture

Figure 1 shows a scan chain consisting of five scan flip-flops. In this example, we assume that the scan flip-flops (SDFF0–SDFF4) consist of a D flip-flop with a multiplexer added at the input—forming a MUX-D scan flip-flop outlined in grey. One input of the MUX acts as the functional input (labeled D0–D4), and the other input serves as the *Scan In* (SI) input. A *Scan Enable* (SE) signal is used as the multiplexer select line. These scan flip-flops also have an enable input (EN). Each flip-flop will only clock the data in when the EN input is asserted. A global *enable* signal dictates whether the flip-flops capture data from the combinational logic (not shown) that feeds into D0–D4 during normal functional operation. De-asserting the EN signal prevents the change of data in the flip-flops. The Scan-Enable signal (SE) is OR'ed with the global enable to ensure that data can be shifted into the flip-flops during test regardless of the value of the global enable. However, the global enable signal must be asserted during the capture cycles of test when SE is deasserted. The global enable signal can be used during functional operation of the circuit to allow this part of the circuit to enter a low-power mode by preventing changes in the flip-flop values.

Figure 2 shows the same five flip-flop scan chain (shaded in grey) from Figure 1 split into two segments using two additional EECB flip-flops (shown in green). Segment 1 consists of two scan cells SDFF0 and SDFF1. Similarly, segment 2 consists of three scan cells SDFF2, SDFF3, and SDFF4. In this figure, each EECB scan flip-flop is connected through the scan chain to the first scan flip-flop of the segment it controls. Unlike the circuit shown in Figure 1, here the global *enable*

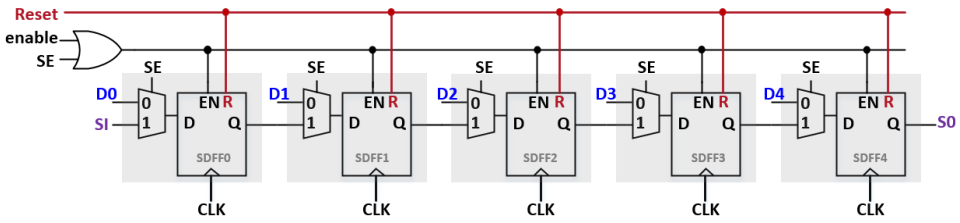

Fig. 1. Schematic design of regular scan chain with enable signal.

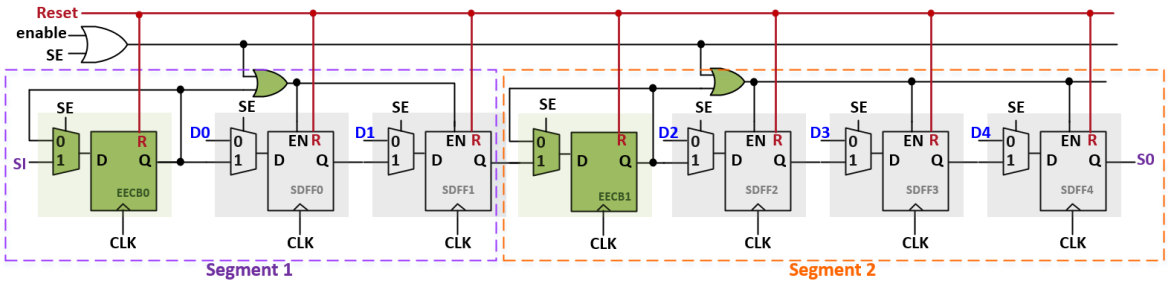

Fig. 2. Schematic design of segmented scan chain.

signal is set to low during test. This will allow the EECB cells to solely control whether or not the scan chain captures data during test. When SE is set to *high*, the segmented scan-chain works as a regular shift register. When SE is set to *low*, the outputs of the OR gates (shaded in green) are determined by the outputs of EECB bits. The value in each EECB flip-flop determines whether the segment it controls will capture a new value or maintain its old value. A logic 0 stored in the EECB flop at the start of a segment leads to a 0 at the output of the OR gate connected to the *EN* pin of the flip-flops in that segment. This has the effect of denying capture and the segment flip-flops retaining their previous value. In the example of Figure 2, using two EECB flops, we can control the two segments independently and have both segments disabled, both segments enabled, or only one of the two segments enabled. In functional mode, the EECBs should be set to 0 to allow the global *enable* to have full control of whether or not the functional flip-flops capture data.

In this example, our approach harnesses the existing *enable* inputs to the flip-flops in the circuit as seen in Figure 2 to allow or deny capture. Alternatively, other approaches such as disabling the flip-flop by gating the clock could be used instead to disable capture during test. The hardware overhead compared to the original chain of Figure 1 is one MUX-D flip-flop and one OR gate per segment, plus the additional routing occurring locally.

In Figure 2, the EECB bits become part of the original scan chain. This allows the ATPG tool to generate the appropriate logic values for the EECB bits to capture data in those segments that are needed to detect targeted faults for a particular test pattern. Furthermore, when low power test patterns are generated, toggling of flip-flop values during shift is kept low. Because segments disabled by EECBs do not capture data, the same low-power values that were shifted into a segment will be shifted out. As a result, this architecture also applies to shift power reduction.

We also found that an ATPG tool is able to generate both stuck-at and Launch on Capture (LOC) transition fault patterns automatically for this segmented scan chain design. In the case of LOC patterns, a segment whose EECB value is 0 is disabled for both capture cycles. The ATPG tool is also able to generate patterns for a design in which an on-chip decompressor is used to fill the segmented scan chains.

IV. EECB Insertion Procedure

To implement the proposed approach, it is necessary to split each scan chain into multiple segments that can be enabled/disabled during capture. More specifically, the following steps are are followed for each circuit studied in this paper.

1) Insert balanced scan chains so that the chain lengths are approximately the same.
2) Split each scan chain evenly into segments.
3) Insert *EECBs* in between the scan segments by modifying the Verilog netlist. Figure 2 shows a case where the scan chain has 2 segments with 2 and 3 cells per segment. One *EECB* cell and a two-input OR gate are inserted before the first scan cell of every segment. The *EECB0* shift-in signal will be the previous shift-in signal of *SDFF0*. In this case, it is the *SI* signal for that scan chain. The output of the *EECB* will fan-out to three paths: feedback to the EECB's mux to allow it to hold value when not shifting, the shift-in signal for the first scan cell of the segment it controls, and one of the inputs into the added OR gate. The other input to the OR gate is the OR of the original *enable* signal and *SE*. In this example, we need two *EECBs* and two additional OR gates per chain.
4) Change the test procedure file. In the ATPG test procedure, the minimum number of shift cycles depends on the number of scan cells in the longest functional chains and the number of *EECBs* that are being added. In this example, the original length of the scan chain is 5. Two *EECBs* are added per chain. The minimum number of

shift cycles should be changed to 5+2=7.

5) Use the ATPG tool to create the on-chip decompressor with the updated test procedure and Verilog netlist.
6) Generate the on-chip decompressor test patterns.

V. Results

To evaluate the effectiveness of our approach, data were collected for four different circuits obtained from opencores.org. The characteristics of these circuits are listed in Table I.

TABLE I
Characteristics of Benchmark Circuits

Circuit	# of scan DFFs	# of scan chains	avg. length of scan chains
des56	312	5	62-63
fm_receiver	509	5	101-102
colorconv	879	5	175-176
fpu_double	5364	5	1072-1073

For each circuit, the steps outlined in Section IV were followed to generate a low power stuck-at test set and a low power transition fault test set using LOC (launch off capture). The goal was to see how much *additional* test power reduction in both shift and capture, above and beyond that which was already obtained by the ATPG low power test pattern set, is possible with this approach. To investigate the effect that different segment lengths may have on the overall power reduction, the process was repeated for different segment lengths.

A. Stuck-At Fault Model Results

In our experiments, low power test patterns that target stuck-at faults in the presence of an on-chip decompressor are created using the procedure in Section IV. The ATPG tool has perfect freedom to decide whether to enable or disable a particular segment during each capture cycle. We then estimate the test power (during both shift and capture cycles) by counting the switching activities.

The results for the first three circuits in Table I are shown in Table II, while the results for circuit *fpu_double* are shown in Table III. This last circuit has significantly longer scan chains, compared to the first three circuits. Therefore, its scan chains are partitioned differently.

In these tables, "PR" denotes power reduction, "total" denotes the percentage of total power reduction during test, "shift" denotes the percentage of shift power reduction during test, and "capture" denotes the percentage of capture power reduction during test.

TABLE II
% Power reduction with different segment lengths for stuck-at faults

circuit name	PR	1/4 chain	1/3 chain	1/2 chain
des56	shift	20.75	21.99	21.91
des56	capture	32.78	33.91	32.33
des56	total	20.91	22.15	22.05
fm_receiver	shift	11.56	11.36	14.68
fm_receiver	capture	16.47	15.00	17.54
fm_receiver	total	11.60	11.39	14.70
colorconv	shift	9.09	7.59	8.95
colorconv	capture	25.94	25.65	26.27
colorconv	total	9.19	7.69	9.05

TABLE III
% Power reduction with different segment lengths for stuck at faults for FPU double

circuit name	PR	1/36 chain	1/12 chain	1/6 chain
fpu_double	shift	35.97	35.82	32.75
fpu_double	capture	43.16	41.72	36.04
fpu_double	total	35.98	35.83	32.75

The results for the four circuits in Table II and Table III show that the DFT architecture presented in Section III can be used to save power during test in both the shift and capture stages for the stuck-at fault model. From our results we see that the largest of our four circuits, *fpu_double*, displays the best power reduction and can achieve up to 35% total test power reduction and up to 43% reduction for total capture power.

B. Transition Fault Model Results

In this section, we repeat the experiments above and analyze power savings when targeting transition faults. With the proposed design, the ATPG tool can automatically determine whether to enable or disable a particular segment for a particular pattern pair when LOC pattern pairs are generated. Results for the four circuits presented in Tables IV and V show power savings in shift and capture as well as total power. We see that our largest circuit *fpu_double* can achieve up to 37% total test power reduction.

TABLE IV
% Power reduction with different segment lengths for transition faults

circuit name	PR	1/4 chain	1/3 chain	1/2 chain
des56	shift	11.62	13.16	23.38
des56	capture	24.59	25.29	33.38
des56	total	11.95	13.47	23.63
fm_receiver	shift	-4.62	9.58	-2.51
fm_receiver	capture	14.78	17.00	5.63
fm_receiver	total	-4.31	9.70	-2.38
colorconv	shift	12.56	12.65	15.41
colorconv	capture	21.90	20.31	25.06
colorconv	total	12.65	10.45	15.50

Table IV shows good power reduction for shift, capture, and overall power for *des56* and *colorconv*. However, for circuit *fm_receiver*, when the chains are segmented to lengths of 1/4 chain and 1/2 chain, the total shift power and total power increased slightly. This is related to a pattern count increase. Specifically, when generating a test pattern set for transition faults for *fm_receiver*, we noticed that the pattern count had increased by about 20% for the 1/4 chain and 1/2 chain scenarios compared to the original circuit without the segmented scan chain. The number of patterns for the 1/3 chain scenario was also higher but not to the same degree as the other two cases. The first set of bars marked "pattern count/original" in Figure 3 shows this increase in pattern count over the original circuit. The other three sets of bars in the figure show the total shift power, total capture power and total power compared to the original circuit.

C. Overhead

Different segment lengths correspond different area overheads as shown in Table VI. In the table, each segment length

TABLE V
% POWER REDUCTION WITH DIFFERENT SEGMENT LENGTHS FOR TRANSITION FAULTS FOR FPU_DOUBLE

circuit name	PR	1/36 chain	1/12 chain	1/6 chain
fpu_double	shift	35.28	37.77	28.33
fpu_double	capture	37.83	30.29	30.06
fpu_double	total	35.28	37.76	28.33

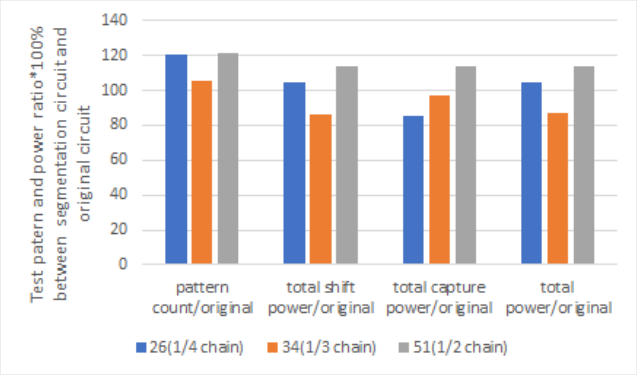

Fig. 3. *fm_receiver* Total test power for transition fault patterns with regard to pattern count for different amounts of scan chain segmentation

L_{seg} is given as both the average number of flops in a segment (e.g. 16) as well as the fractional portion of a chain of which a segment consists (e.g. 1/4 chain). Each segment requires an additional MUX-D flip-flop and an OR gate to be inserted in between the segments. In this paper, we extract the area overhead after synthesizing and mapping the circuits to a standard cell library. The global enable signal was included for all flops. As the segment length gets larger, the area overhead gets smaller.

TABLE VI
% AREA OVERHEAD WITH DIFFERENT SEGMENT LENGTHS

des56	L_{seg}	16(1/4 chain)	21(1/3 chain)	32(1/2 chain)
	A_o	5.2	4.65	4.13
fm_receiver	L_{seg}	26(1/4 chain)	34(1/3 chain)	51(1/2 chain)
	A_o	3.22	2.92	2.84
colorconv	L_{seg}	44(1/4 chain)	60(1/3 chain)	90(1/2 chain)
	A_o	4.05	3.69	3.49
fpu_double	L_{seg}	30(1/36 chain)	90(1/12 chain)	180(1/6 chain)
	A_o	2.44	2.31	2.24

VI. CONCLUSIONS AND FUTURE WORK

Significant switching activity reduction can be achieved by disabling capture of selected scan chain segments during test. For our largest circuit, *fpu_double*, using a chain length of 180 (1/6 chain), we can achieve total power savings of approximately 35% while incurring only 2.4% area overhead. We expect the approach to scale well to even larger circuits that have a high percentage of don't care values in their test pattern sets.

A significant advantage of the proposed approach is that the ATPG tool is able to generate test patterns that include the appropriate EECB values automatically without significant post processing. It is also able to generate a LOC test pattern set automatically to target transition faults. This was not possible with our previously proposed approach. Furthermore, in most cases, multiple segment lengths can lead to good power reduction for each circuit—indicating that good trade-offs between power reduction and area overhead are possible.

REFERENCES

[1] A. Bosio, P. Girard, and A. Virazel, "Test of low power circuits: Issues and industrial practices," in *2016 IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, Dec 2016, pp. 524–527.

[2] K. M. Butler, J. Saxena, A. Jain, T. Fryars, J. Lewis, and G. Hetherington, "Minimizing power consumption in scan testing: pattern generation and dft techniques," in *Intl. Test Conf.(ITC)*, Oct 2004, pp. 355–364.

[3] P. Girard, L. Guiller, C. Landrault, S. Pravossoudovitch, and H. J. Wunderlich, "A modified clock scheme for a low power bist test pattern generator," in *IEEE VLSI Test Symposium*, April 2001, pp. 306–311.

[4] S. Wu, L. Wang, L. Yu, H. Furukawa, X. Wen, W. Jone, N. A. Touba, F. Zhao, J. Liu, H. Chao, F. Li, and Z. Jiang, "Logic bist architecture using staggered launch-on-shift for testing designs containing asynchronous clock domains," in *2010 IEEE 25th International Symposium on Defect and Fault Tolerance in VLSI Systems*, Oct 2010, pp. 358–366.

[5] S. Gupta, B. Bhaskaran, S. Sarangi, A. Abdollahian, and J. Dworak, "A novel graph coloring based solution for low-power scan shift," in *2019 IEEE 37th VLSI Test Symposium (VTS)*, 2019, pp. 1–6.

[6] D. Xiang, X. Wen, and L. Wang, "Low-power scan-based built-in self-test based on weighted pseudorandom test pattern generation and reseeding," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 25, no. 3, pp. 942–953, March 2017.

[7] X. Wen, Y. Yamashita, S. Morishima, S. Kajihara, , K. K. Saluja, and K. Kinoshita, "Low-capture-power test generation for scan-based at-speed testing," in *Intl. Test Conf.*, Nov 2005, pp. 10 pp.–1028.

[8] E. K. Moghaddam, J. Rajski, S. M. Reddy, X. Lin, N. Mukherjee, and M. Kassab, "Low capture power at-speed test in edt environment," in *2010 IEEE International Test Conference*, Nov 2010, pp. 1–10.

[9] D. Czysz, M. Kassab, X. Lin, G. Mrugalski, J. Rajski, and J. Tyszer, "Low-power scan operation in test compression environment," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 28, no. 11, pp. 1742–1755, Nov 2009.

[10] S. Kajihara, K. Ishida, and K. Miyase, "Test vector modification for power reduction during scan testing," in *Proceedings 20th IEEE VLSI Test Symposium (VTS 2002)*. IEEE, 2002, pp. 160–165.

[11] J. T. Tudu, E. Larsson, V. Singh, and V. D. Agrawal, "On minimization of peak power for scan circuit during test," in *IEEE European Test Symposium*, May 2009, pp. 25–30.

[12] R. Sankaralingam, R. R. Oruganti, and N. A. Touba, "Static compaction techniques to control scan vector power dissipation," in *Proceedings 18th IEEE VLSI Test Symposium*. IEEE, 2000, pp. 35–40.

[13] M. Filipek, Y. Fukui, H. Iwata, G. Mrugalski, J. Rajski, M. Takakura, and J. Tyszer, "Low power decompressor and prpg with constant value broadcast," in *2011 Asian Test Symposium*, Nov 2011, pp. 84–89.

[14] D. Czysz, G. Mrugalski, N. Mukherjee, J. Rajski, P. Szczerbicki, and J. Tyszer, "Deterministic clustering of incompatible test cubes for higher power-aware edt compression," *IEEE Trans on Computer-Aided Design of Integrated Circuits & Systems*, vol. 30, no. 8, pp. 1225–1238, 2011.

[15] L. Lee, C. He, and W. Tseng, "Deterministic atpg for low capture power testing," in *2012 13th International Workshop on Microprocessor Test and Verification (MTV)*, Dec 2012, pp. 24–29.

[16] R. Shaikh, P. Wilson, K. Agarwal, H. V. Sanjay, R. Tiwari, K. Lath, and S. Ravi, "At-speed capture power reduction using layout-aware granular clock gate enable controls," in *Intl. Test Conference*, Oct 2014, pp. 1–10.

[17] Z. You, T. Iwagaki, M. Inoue, and H. Fujiwara, "A low power deterministic test using scan chain disable technique," *IEICE Transactions on Information and Systems*, vol. E89D, 06 2006.

[18] Z. You, J. Huang, M. Inoue, J. Kuang, and H. Fujiwara, "Capture in turn scan for reduction of test data volume, test application time and test power," in *IEEE Asian Test Symposium*, Dec 2010, pp. 371–374.

[19] Y. Sun, H. Jiang, L. Ramakrishnan, M. Segal, K. Nepal, J. Dworak, T. Manikas, and R. I. Bahar, "Test architecture for fine grained capture power reduction," in *2019 26th IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, 2019, pp. 558–561.