

# David W. Matula

February, 2017

Cruse C. and Marjorie F. Calahan Centennial Chair of Engineering and  
Professor of Computer Science and Engineering  
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Deborah (b.5/8/68)  
Theodore (b.7/23/69)  
Thaddeus (b.7/13/78)

Birthdate: 06 Nov. 1937

## **EDUCATION:**

Ph.D. University of California, Berkeley, 1966.  
B.S. Washington University, St. Louis, 1959.  
College Honors: Tau Beta Pi, Sigma Xi, Final Honors, Woodrow Wilson Fellow.

## **EMPLOYMENT:**

### **Primary Positions:**

Southern Methodist University (Comp. Sci. and Eng.)	
Cruse C. and Marjorie F. Calahan Centennial Chair of Engineering	Mar 2016 - present
Professor	Aug 1974 - present
Department Chairman	Aug 1974 - June 1979
Department Chairman ad interim	Aug 1988 - Aug 1989
Washington University (Ap. Math. And Comp. Sci.)	
Assistant Professor	Feb 1966 – Aug 1969
Associate Professor (tenured)	Sept 1969 – Aug 1974
University of California, Berkeley (Comp. Ctr./half-time)	Sept 1960 – Jan 1966
Monsanto Company (Research Center/summers only)	1957 – 1964

### **Visiting Positions:** (3 months or more)

University of Odense, Denmark, Visiting Professor	Sept 1989 – July 1990
% P. Kornerup	
University of Frankfurt, West Germany, Visiting Professor	May – July 1986
% C. P. Schnoor	
Aarhus University, Denmark, Visiting Professor	Aug 1980 – Jan 1981
% P. Kornerup	
Stanford University, Visiting Professor	Feb – July 1980
% D. E. Knuth	
Naval Postgraduate School, Distinguished Visiting Professor	April – June 1978
% G. Bradley	
University of Karlsruhe, Visiting Professor	May – Aug 1974
% U. Kulisch	
University of Texas, Austin, Research Scientist	Feb – June 1973
% R. T. Gregory	

**Consulting:** Cyrix Corporation/National Semiconductor/AMD, 1988 – 2005. (Work involved floating point unit architecture and has led to thirteen patents awarded.)

**RESEARCH INTERESTS:**

- Algorithm Engineering
- Network Science / Graph Theory
- Computer Arithmetic
- Cluster Analysis/Social Networks

**PROFESSIONAL OFFICES AND ACTIVITIES:**

Editorial Board, (founding member), *Random Structures and Algorithms* (1989-2001).  
Editorial Board, (founding member), *Journal of Classification* (1984-1991).  
Associate Editor, *ORSA Journal of Computing* (1987-1989).  
Editorial Board, *IEEE Trans on Comp* (1992-1994).  
Founding Officer (Sec.- Treas) of the Special Interest Committee/Group on Computer Science Education of the ACM (1969-1973).  
Guest Editor, *IEEE Trans on Comp* 41, No. 8, (Sp Is on Comp Arith), Aug. 1992.  
Editor: *Proceedings of the 10<sup>th</sup> IEEE Symposium on Computer Arithmetic* (with Peter Kornerup), IEEE Computer Society Press, Los Alamedas, 1991, 282 pp.  
Program Chairman: 3<sup>rd</sup> IEEE Symposium on Computer Arithmetic, Dallas, Nov. 1975.  
Program Co-Chairman: 10<sup>th</sup> IEEE Symposium on Computer Arithmetic, Grenoble, June 1991.  
General Chairman: 15<sup>th</sup> IEEE Symposium on Computer Arithmetic, Vail, June, 2001.  
General Chairman: 21<sup>st</sup> IEEE Symposium on Computer Arithmetic, Austin, April, 2013.

**PRINCIPAL UNIVERSITY SERVICE:**

Member: Search committee for the 9th President of Southern Methodist University, Dec. 1986 - May 1987.

**RESEARCH GRANTS: Principle Investigator**

SRC, *Development of Fast Divide Algorithms and Decimal Arithmetic for Next Generation Microprocessors*, \$120,000 (+matching), July 1, 2009-June 30, 2012.  
SRC, *Table Assisted Implementations of Integer and Floating Point ALU's for Low Power SIMD Scientific and Multi-Media Processors*, \$230,000, Feb. 1, 2006-June 30, 2008.  
HP, *Network Algorithms and Optimization*, \$10,000, March-April, 2007  
SRC, *LowPower Table Assisted SIMD Floating Point for Multi-Media Processors*, \$74,995; Jan-Dec 2005.  
Cyrix, *Design of a Next Generation Fl. Pt. Unit: Multimedia Extensions*, \$185,379; Jan 1996-Dec 1997.  
Cyrix, *Design of a Next Generation Floating Point Unit for the x86*, \$181,457; May 1993-Dec 1995.  
THECB, *Integrating Virtual Reality, DSP and Vector Processing into a PC*, \$174,234; Jan 1994-Dec 1995.  
Cyrix, *Standard for Floating Point Units*, \$8,000; May 1992-April 1993.  
Cyrix, *Standard for Floating Point Units*, \$10,000; Jan 1991-Dec 1991.  
Texas Instruments, *Design of Arithmetic Systems*, \$25,000; Jan 1990-Dec 1990.  
Cyrix, *Highly Parallel Floating Point Units*, \$6,000; Jan 1989-Dec 1989.  
NSF, *Foundations of Finite Precision Rational Arithmetic*, \$145,413; April 1984-Oct 1988.  
NSF, *Foundations of Finite Precision Arithmetic*, \$95,056; Aug 1980-Dec 1983.  
NSF, *Foundations of Finite Precision Arithmetic*, \$44,369; Aug 1977-July 1979.  
NSF, *Foundations of Finite Precision Arithmetic*, \$14,000; April 1975-June 1976.  
NSF, *"Theory and Computational Efficiency of Several Graph Theoretic Approaches to Cluster Analysis"*, \$49,300; Sept 1973-Aug 1975.  
NSF, *Foundations of Finite Precision Arithmetic*, \$42,900; Jan 1973-Dec 1974.

**Proposals Under Review:**

E. V. Olinick and D. W. Matula, Co.P.I., NSF, *A Network Flow Duality Foundation for Hierarchical Cluster Analysis*, \$391,811. (submitted Sept, 2016)

**Ph. D. DISSERTATIONS DIRECTED:**

M.T. Panu, “*Generalized Reciprocal Function Algorithms for Multiplicative Division and ALU Design*”, 2014.

D. Mahjoub, “*Efficient Redundant Backbones for Coverage and Routing in Wireless Sensor Networks*”, 2011.

I. M. Derici, “*Random Geometric Graphs, their Properties and Applications on the Plane, Sphere and Torus*”, 2010.

C. Mann, “*Extensions of Maximum Concurrent Flow to Identify Hierarchical Community Structure and Hubs in Networks*”, 2008.

A. Fit Florea, “*Extending Hardware Support for Arithmetic Modulo  $2^k$* ”, 2005.

L. McFearin, “*A p-Bit Model of Binary Floating Point Division and Square Root with Emphasis on Extremal Rounding Boundaries*”, 2002

C. Iordache, “*Rounding Standards and Interpolative Algorithms for Reciprocal, Division, Square Root and Square Root Reciprocal*”, 1999

M. Iridon, “*Regular Triangulated Toroidal Graphs with Applications in Cellular and Interconnection Networks*”, 1999

C. N. Lyu, “*Micro-Architecture of a Pipelined Floating-Point Execution Unit*”, 1995

D. Das Sarma, “*Highly Accurate Initial Reciprocal Approximation for High Performance Division Algorithms*”, 1995

W. Cai, “*Fast Algorithms to Compute Edge Connectivity of Undirected Graphs*”, 1995

C. Yang, “*A Multi-Layer Design and Load Sharing Algorithm for Personal Communication Networks*,” 1991

S. N. Parikh, “*An Architecture for a Rational Arithmetic Unit*”, 1988

F. Shahrokhi, “*The Maximum Concurrent Flow Problem*”, 1986

W.H. Day, “*Flat Cluster Methods*”, 1975

W.E. Wright, “*A Formalization of Cluster Analysis, and Gravitational Clustering*”, 1972

R.M. Simon, “*The Reliability of Multi-State Systems Subject to Cannibalization*”, 1969

**Ph. D. DISSERTATIONS IN PROGRESS (anticipated completions):**

Z. Chen (2017), F. Vilas (2018), J. Chavez (2018).

**M. S. Thesis in Progress:**

A. J. Rao (2017), A. McCarthy (2017)

**BOOKS:**

P. Kornerup, and D. W. Matula, "Finite Precision Number Systems and Arithmetic", Cambridge University Press, 2010, 699pp.

**PATENTS:**

21. "Method and Apparatus for Integer Conversion Using the Discrete Logarithm and Modular Factorization", with A. Fit-Florea, U.S. Patent #8,060,550, Nov. 2011.
20. "Determining A Table Output Of A Table Representing A Hierarchical Tree For An Integer Valued Function" with A. Fit-Florea, L.Li, M.A. Thornton. US. Patent #7,962,537, June. 2011.
19. "Apparatus and Method for Providing Higher Radix Redundant Digit Lookup Tables for Recoding and Compressing Function Values", with W. S. Briggs, U.S. Patent #7,543,008, June. 2009.
18. "Arithmetic Processor Utilizing Multi-Table Look Up to Obtain Reciprocal Operands", with W.S. Briggs, U.S. Patent #7,346,642, Mar. 2008.
17. "Higher Radix Multiplier with Simplified Partial Product Generator", with P.M. Seidel and L.D. McFearin, U.S. Patent # 7,194,498, Mar. 20, 2007.
16. "Apparatus and Method for Minimizing Accumulated Rounding Errors in Coefficient Values in a Lookup Table for Interpolating Polynomials", U.S. #6,978,289, Dec. 2005.
15. "Apparatus and Method for Providing Higher Radix Redundant Digit Lookup Tables for Recording and Compressing Function Values", with W. S. Briggs, U.S. Patent #6,938,062, Aug. 2005.
14. "Method and Apparatus for Performing Division and Square Root Functions Using a Multiplier and a Multipartite Table", with C. Iordache, U.S. Patent # 6,782,405 B1, Aug. 2004.
13. "Channel Assignment Selection Reducing Call Blocking and Call Cutoff in a Cellular Communication System", with C.Yang, U.S. Patent #5,896,573, April, 1999.
12. "Table Compression Using Bipartite Tables", with D. Das Sarma, U.S. Patent #5,862,059, Jan. 1999.
11. "Early Detection of Overflow and Exceptional Quotient/Remainder Pairs for Nonrestoring Twos Complement Division", U.S. Patent # 5,675,528, Oct. 1997.
10. "Numeric Processor Including a Multiply-Add Circuit for Computing a Succession of Product Sums Using Redundant Values without Conversion to Nonredundant Format", with W. S. Briggs, U.S. Patent # 5,659,495, Aug.1997.
9. "A Multilayered Arrangement for Load Sharing in a Cellular Communications System", with C. Yang, U.S. Patent # 5,633,915, May 1997.
8. "Early Signaling of No-Overflow for Nonrestoring Twos Complement Division", U.S. Patent #5,615,113, March 1997.
7. "Method and Apparatus for Prescaled Division", with W. S. Briggs, U.S. Patent #5, 475, 630, Dec.1995.
6. "Method and Apparatus for Performing Division Using a Rectangular Aspect Ratio Multiplier", with W. S. Briggs, U. S. Patent #5,307,303, April 1994.
5. "Rectangular Array Signed Digit Multiplier", with W. S. Briggs, U. S. Patent # 5,184,318, Feb. 1993.
4. "Method and Apparatus for Performing the Square Root Function Using a Rectangular Aspect Ratio Multiplier", with W. S. Briggs and T. Brightman, U.S. Patent #5,159,566, Oct. 1992.
3. "Signed Digit Multiplier", with W. S. Briggs, U.S. Patent #5,144,576, Sept. 1992.
2. "Method and Apparatus for Performing the Square Root Function Using a Rectangular Aspect Ratio Multiplier", with W. S. Briggs and T. Brightman, U.S. Patent #5,060,182, Oct. 1991.
1. "Method and Apparatus for Performing Division Using a Rectangular Aspect Ratio Multiplier", W. S. Briggs and T. Brightman, U.S. Patent #5,046,038, Sept. 1991.

**KEYNOTE PRESENTATIONS TO INTERNATIONAL CONFERENCES (last 15 years)**

“Freezing Arithmetic Algorithms into Foundational Number Representation Theorems”, Keynote Talk, Numeration 2016, Prague, Czech Republic, May 23-27, 2016.

“Division: Improved Algorithms and Implementations”, Keynote Talk, 8<sup>th</sup> Conference on Real Numbers and Computers (RNC 8), Santiago de Compostela, Spain, July 7-9, 2008 (<http://www.ac.usc.es/rnc8/>)

“Foundations of Higher Radix Numeric Computation”, Keynote Talk, 38<sup>th</sup> International Symposium on Multiple Valued Logic, IEEE, Dallas, TX, May 22-24, 2008 (<http://engr.smu.edu/ismvl08/>)

“Arithmetic Illiteracy: Algorithms We Were Not Told We Knew”, Plenary Talk, NSF funded Workshop on Algorithms, Combinatorics, and Geometry, Denton, TX, November 29-December 1st, 2007 (<http://acg.unt.edu/index.php>)

“Computer Arithmetic – An Algorithm Engineer’s Perspective”, Keynote Talk, 16<sup>th</sup> Symposium on Computer Arithmetic, IEEE, Santiago de Compostela, Spain, June 2003.

**Conference Presentations in 2016 (refereed extended abstract):**

D. W. Matula and E. V. Olinick, “A Network Flow Duality Foundation for Hierarchical Cluster Analysis”, SIAM Workshop on Network Science, Boston, July 15-16, 2016.

**PUBLICATIONS:****Top 10 Cited Publications (Google Scholar):**

1. F. Shahrokhi and D. W. Matula, “The Maximum Concurrent Flow Problem”, *J.A.C.M.*, 37, 1990, 318-334. *Cited by 442.*
2. D. W. Matula and R. R. Sokal, “Properties of Gabriel Graphs Relevant to Geographic Variation Research and the Clustering of Points in the Plane”, *Geographical Analysis*, 12, 1980, 205-222. *Cited by 328.*
3. D. W. Matula, G. Marble and J.D. Isaacson, “Graph Coloring Algorithms”, in *Graph Theory and Computing*, R. Read, ed., Academic Press, New York, 1972, 109-122. *Cited by 286.*
4. D. W. Matula and L. Beck, “Smallest Last Ordering and Clustering and Graph Coloring Algorithms”, *J.A.C.M.*, 30, 1983, 417-427. *Cited by 255.*
5. D. W. Matula and D. Das Sarma, “Faithful Bipartite ROM Reciprocal Tables”, *Proc. 12<sup>th</sup> Sym. on Comp. Arith.*, IEEE Cat. #95CB35822, 1995, 17-28. *Cited by 191.*
6. D. W. Matula, “Determining Edge Connectivity in  $O(nm)$ ”, *Proc. 28<sup>th</sup> IEEE FOCS*, 1987, 249-251. *Cited by 116.*
7. D. W. Matula, “Graph Theoretic Techniques for Cluster Analysis Algorithms”, in *Classification and Clustering*, J. Van Ryzin, ed., Academic Press, New York, 1977, 95-129. *Cited by 119.*
8. D. W. Matula, “Subtree Isomorphism in  $O(n^{5/2})$ ”, *Ann. Dis. Math.* 2, 1978, 91-106. *Cited by 113.*
9. D. W. Matula, “The Largest Clique Size in a Random Graph” Tech Report CS 7608, *Department of Computer Science and Engineering*, Southern Methodist University, 1976. *Cited by 110.*
10. D. W. Matula, “On the Complete Subgraphs of a Random Graph”, *Proc. of the Second Chapel Hill Conference on Combinatorial Mathematics and Its Applications*, University of North Carolina, Chapel Hill, 1970, 356-369. *Cited by 100.*

**REFEREED JOURNAL AND CONFERENCE PUBLICATIONS:**

128. "A Compact Linear Programming Formulation for the Maximum Concurrent Flow Problem", with T. J. Kratz, E. V. Olinick and Y. Dong, *Networks*, vol. 65, 2015, pp. 68-87.
127. "Multiplicative Division Employing Independent Factors" with J. Y. Zhang and M. T. Panu, *IEEE Trans. on Computers*, vol. 64, 2015, pp. 2012-2019.
126. "Constructing Efficient Rotating Backbones in Wireless Sensor Networks using Graph Coloring" with D. Mahjoub, *Computer Communications Journal (Elsevier), Special Issue on Wireless Sensor and Robot Networks: Algorithms and Experiments*, 2012, pp. 1086-1907.
125. "A Prescale-Lookup-Postscale Additive Procedure for Obtaining a Single Precision Ulp Accurate Reciprocal", with M. T. Panu, *Proc. IEEE 20<sup>th</sup> Symposium on Computer Arithmetic*, 2011.
124. "Approximating the Independent Domatic Partition Problem in Random Geometric Graphs – An Experimental Study", with D. Mahjoub and A. Leskovskaya, *Proc. of Canadian Conference on Computational Geometry (CCCG)*, 2010, pp. 195-198. Extended version available at <http://www.cs.umanitoba.ca/cccg2010/electronicProceedings/paper84.pdf>
123. "Building (1- $\epsilon$ ) Dominating Set Partitions as Backbones in Wireless Sensor Networks using Distributed Graph Coloring", with D. Mahjoub, *Proc. of the 6<sup>th</sup> IEEE International Conference on Distributed Computing in Sensor Systems (DCOSS)*, 2010, pp. 144-157.
122. "Employing (1- $\epsilon$ ) Dominating Set Partitions as Backbones in Wireless Sensor Networks", with D. Mahjoub, *Proc. of the 11<sup>th</sup> Workshop on Algorithm Engineering and Experiments (ALENEX)*, 2010, pp. 98-112.
121. "A Low Power High Performance Radix-4 Approximate Squaring Circuit", with S. R. Datla, M. A. Thornton, *Proc. of ASAP*, 2009, pp. 91-97
120. "Higher Radix Squaring Operations Employing Left-to-Right Dual Recoding", *Proc. IEEE 19<sup>th</sup> Symposium on Computer Arithmetic*, 2009, pp. 39-47
119. "Experimental Study of Independent and Dominating Sets in Wireless Sensor Networks Using Graph Coloring Algorithms", with D. Mahjoub, *Proc. of International Conference on Wireless Algorithms, Systems and Applications WASA*, 2009, pp. 32-42.
118. "A Discrete Logarithm Number System for Integer Arithmetic Modulo  $2^k$ : Algorithms and Lookup Structures", with A. Fit-Florea, L. Li, M.A. Thornton, *IEEE Trans. Computers*, vol. 58(2), 2009, pp. 163-174).
117. "The Use of Sparsest Cuts to Reveal the Hierarchical Community Structure of Social Networks", with C. F. Mann, E. V. Olinick; *Social Networks*, vol. 30, 2008, pp. 223-234).
116. "Quantum Logic Implementation of Unary Arithmetic Operators", with L. Spenner; M. A. Thornton; D. M. Miller, *IEEE International Symposium on Multiple-Valued Logic (ISMVL 2008)*, pp. 202-207.
115. "Multilevel Variable Length Shifter Design for an Iterated Shift-and-Add Product Operation", with J. Moore, M.A. Thornton, D. W. Matula, *Proceedings of the IEEE Region 5 Technical Conference*, April 20-22, 2007, pp. 234-238
114. "Performance Evaluation of a Novel Table Lookup Method and Architecture with Application to 16-bit Integer Functions", with L. Li, A. Fit-Florea, and M. A. Thornton, *IEEE International Conference on Application-Specific Systems, Architectures, and Processors (ASAP)*, September 11-13, 2006, pp. 99-104.

113. "A Digit Serial Algorithm for the Integer Power Operations", with L. Li and M.A. Thornton, *ACM/IEEE Great Lakes Symposium on VLSI (GLSVLSI)*, April 20-May 2, 2006, pp. 302-307.
112. "A Formal Method and Efficient Traversal Algorithm for Generating Testbenches for Verification on IEEE Standard Floating Point Division", with L. D. McFearin, *Proc. DATE 2006*, pp. 1134-1138.
111. "Hardware Implementation of an Additive Bit-Serial Algorithm for the Discrete Logarithm Modulo  $2^k$ ", with L. Li, A. Fit-Florea, M. A. Thornton, *Proc. ISVLSI 2005*, pp. 130-135.
110. "Single Precision Reciprocal by Multipartite Table Lookup", with P. Kornerup, *Proc. IEEE Symposium on Computer Arithmetic 2005*, pp. 240-248.
109. "Table Lookup Structures for Multiplicative Inverses Modulo  $2^k$ ", with A. Fit-Florea and M. Thornton, *Proc. IEEE Symposium on Computer Arithmetic 2005*, pp. 156-163.
108. "Secondary Radix Recodings for Higher Radix Multipliers", with P. M. Seidel, and L. D. Mc Fearin, *IEEE Trans. Computers.*, vol. 54(2), 2005, pp. 111-123.
107. "Additive Bit-serial Algorithm for the Discrete Logarithm Modulo  $2^k$ ", with A. Fit-Florea and M. Thornton, *IEE Electronics Letters*, January, 2005, pp. 57-59.
106. "Addition-based Exponentiation Modulo  $2^k$ ", with A. Fit-Florea and M. Thornton, *IEE Electronics Letters*, January, 2005, pp. 56, 57.
105. "Determining All Pairs Edge Connectivity of a 4-regular Graph in  $O(|V|)$ ", with A. Fit-Florea, *Proc. of the ACS/IEEE 2005 International Conference on Computer Systems and Applications, AICCSA 2005*, pp.15.
104. "A Digit-Serial Algorithm for the Discrete Logarithm Modulo  $2^k$ ", with A. Fit-Florea, *Proc. ASAP, IEEE*, 2004, pp. 236-246.
103. "Prescaled Integer Division", with A. Fit-Florea, *Proc. 16<sup>th</sup> Symp. Comp.Arith., IEEE*, June 2003, pp. 63-68.
102. "A  $pxp$  Bit Fraction Model of Binary Floating Point Division and Extremal Rounding Cases", with L. D. McFearin, *J.Th. Comp. Sci.*, 291, 2003, pp. 159-182.
101. "Further Reducing the Redundancy of a Notation over a Minimally Redundant Digit Set", with M. Daumas, *JVLSI* vol 33, 2003, pp. 7-18.
100. "A 6-Regular Torus Graph Family with Applications to Cellular and Interconnection Networks", with M. Iridon, *JGAA*, vol 6, 2002, pp. 373-404.
99. "Evaluating Products of Non Linear Functions by Indirect Bipartite Table Lookup", with A. Fit-Florea, and L. D. McFearin, *Proc. ASAP, IEEE*, 2002, pp. 120-129.
98. "Selecting Test Suites for IEEE Standard Floating Point Division", with L.D. McFearin, *Proc.IEEE International Conf. on Computer Design*, Sept. 2001, pp. 89-96.
97. "Binary Multiplication Radix-32 and Radix-256", with P.-M. Seidel, and L.D. McFearin, *Proc.15<sup>th</sup> Symp. Comp. Arith., IEEE* June 2001, pp. 23-32.
96. "Generation and Analysis of Hard to Round Test Cases for Binary Floating Point Division", with L.D. McFearin, *Proc. 15<sup>th</sup> Symp. Comp. Arith., IEEE* June 2001, pp. 119-126.

95. "Improved Table Lookup Algorithms for Postscaled Division", *Proc. 15<sup>th</sup> Symp. Comp. Arith, IEEE* June 2001, pp. 101-108.
94. "A Graph Theoretic Approach for Channel Assignment in Cellular Networks", with M. Iridon, and C. Yang, *Wireless Networks Journal*, vol 7, 2001, pp. 567-574.
93. "A Booth Multiplier Accepting Both a Redundant or a Non Redundant Input with No Additional Delay", with M. Daumas, *Proc. ASAP*, 2000, pp. 205-214.
92. "Improving Goldschmidt Division, Square Root, and Square Root Reciprocal", with M.D. Ercegovic, L. Imbert, J.M. Muller, and G. Wei, *IEEE Trans. on Comp*, vol 49, 2000 pp. 759-763.
91. "Number Theoretic Foundations of Binary Floating Point Division with Rounding", with L.D. McFearin, *Proc. RNC4*; April 2000, pp. 39-60.
90. "An IEEE Compliant Floating – Point Adder that Conforms with the Pipelined Packet-Forwarding Paradigm", with A.M. Neilsen, C.N. Lyu, and G. Even, *IEEE Trans. on Comp.*, vol 49, 2000, pp. 33-47.
89. "Analysis of Reciprocal and Square Root Reciprocal Instructions in the AMD K6-2 Implementation of 3D Now!", with C. Ioradache, *ENTCS*, vol. 24, Aug. 1999.
88. "On Infinitely Precise Rounding for Division, Square Root, Reciprocal, and Square Root Reciprocal", with C. Iordache, *Proc. 14<sup>th</sup> Symp. on Comp. Arith., IEEE Car.* #99CB36336, 1999, pp. 233-240.
87. "Performance Analysis of A Graph Model for Channel Assignment in a Cellular Network", with H. Cankaya, and M. Iridon, *Proc. of IEEE COMPSAC'99*, 1999, pp.239-240.
86. "Symmetric Cellular Network Embeddings on a Torus", with M. Iridon, *IEEE, Proc. of ICCCN*, 1998, pp. 732-736.
85. "Faithful Interpolation over Reciprocal Tables", with D. Das Sarma, *Proc. 13<sup>th</sup> IEEE Symp. on Comp. Arith., IEEE Cat# 97CB36091*, 1997, pp. 82-91.
84. "Pipelined Packet-Forwarding Floating Point: I. Foundations and a Rounder", with A. M. Nielsen, *Proc. 13<sup>th</sup> IEEE Symp. On Comp. Arith., IEEE Cat# 97CB36091*, 1997, pp. 140-147.
83. "Pipelined Packet-Forwarding Floating Point: II. An Adder", with A.M.Nielsen, C.N.Lyu and G.E.Even, *Proc. 13<sup>th</sup> Symp. On Comp. Arith., IEEE Cat# 97CB36091*, 1997, pp. 148-155.
82. "Validating Roundings of Dot Products", with M. Daumas, *IEEE Trans. on Computers*, 46, 1997.
81. "Hardware Reciprocal Table Compression/Decompression Techniques", with D. Das Sarma, in *Scientific Computing and Validated Numerics, Akademik Verlag*, 1995, pp. 11-17.
80. "LCF: A Lexicographic Binary Representation of the Rationals", with P. Kornerup, *J. U. C. S. I*, 1995, 480-499.
79. "Faithful Bipartite ROM Reciprocal Tables", with D. Das Sarma, *Proc. 12<sup>th</sup> Sym. on Comp. Arith., IEEE Cat. #95CB35822*, 1995, 17-28.
78. "Redundant Binary Booth Recoding", with C. N. Lyu, *Proc. 12<sup>th</sup> Sym. on Comp. Arith., IEEE Cat# 95CB35822*, 1995, 50-57.
77. "Partitioning by Maximum Adjacency Search of Graphs", with W. Cai, in *Partitioning Data Sets*, I.J. Cox, P. Hansen, B. Julesz, ed., DIMAS 19, AMS, Providence, 1995, 55-63.



76. "Rounding of Floating Point Intervals", with M. Daumas, *Interval Computations*, No.4, 1994, 28-45.
75. "Measuring the Accuracy of ROM Reciprocal Tables", with D. Das Sarma, *IEEE Trans. on Comp.*, 43, 1994, 932-940.
74. "Measuring the Accuracy of ROM Reciprocal Tables", with D. Das Sarma, *Proc. 11<sup>th</sup> Sym. on Comp. Arith.*, IEEE Cat# 93CH3324-1, 1993, 95-102.
73. "Design of a Fast Validated Dot Product Operation", with M. Daumas, *Proc. 11<sup>th</sup> Sym. on Comp. Arith.*, IEEE Cat# 93CH3324-1, 1993, 62-69.
72. "A 17 x 69 Bit Multiply and Add Unit with Redundant Binary Feedback and Single Cycle Latency", with W. S. Briggs, *Proc. 11<sup>th</sup> Sym. On Comp. Arith.*, IEEE Cat# 93CH3324-1, 1993, 163-170.
71. "A Linear Time  $(2+\epsilon)$  Approximation Algorithm for Edge Connectivity". *Proc. 4<sup>th</sup> ACM-SIAM Sym. on Dis. Algorithms*, 1993, pp. 500-504.
70. "Semantics for Exact Floating Point Operations", with G. Bohlender, P. Kornerup, and W. Walter, *Proc. 10<sup>th</sup> Sym. on Comp.Arith.*, IEEE Cat# 91CH3015-5, 1991, 22-26.
69. "A Redundant Binary Euclidean GCD Algorithm", with S. N. Parikh, *Proc. 10<sup>th</sup> Sym. on Comp. Arith.*, IEEE Cat# 91CH3015-5, 1991, 220-225.
68. "An Algorithm for Redundant Binary Bit-Pipelined Rational Arithmetic", with P. Kornerup, *IEEE Trans. on Comp.*, C-39, 1990, 1106-1115.
67. "The Maximum Concurrent Flow Problem", with F. Shahrokhi, *J.A.C.M.*, 37, 1990, 318-334.
66. "Sparsest Cuts and Bottlenecks in Graphs", with F. Shahrokhi, *Discrete Applied Mathematics*, 1990, 113-123.
65. "An Expose and Merge Algorithm and the Chromatic Number of a Random Graph", with L. Kucera, in *Random Graphs '87*, M. Karonski, J. Jaworski, and A. Rucinski, ed., Wiley, New York, 1990, 175-187.
64. "Exploiting Redundancy in Bit-Pipelined Rational Arithmetic", with P. Kornerup, *Proc. 9<sup>th</sup> IEEE Sym. on Comp. Arith.*, IEEE Cat# 89CH2757-3, 1989, 119-126.
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