CSE/EE 5/7385 Microcontroller Architecture and Interfacing

HOMEWORK 6

1. Slide number 26 in the class notes entitled "Memory System Architecture" in week 12 shows a simple memory interface. You are to design a different memory interface that has the same architecture as slide 26, but uses different memory chips. You will use the following memory devices:

- Eight (8) SRAM chips that are 8M×4 bits capacity and have !oe and !we control signals identical to the SRAM chips on slide 26. (Note: !oe means that the 'output enable' signal is active low and !we means that the 'write enable' signal is active low.)

- Four (4) ROM chips that are 1M×8 bits capacity and have a !oe active-low output enable input.

a) The SRAM chips each have a bidirectional data bus of *m* pins and a unidirectional address bus of *n* pins. What is the value of *m* and *n*?

m = _____ *n* = _____

b) The ROM chips each have a bidirectional data bus of *m* pins and a unidirectional address bus of *n* pins. What is the value of *m* and *n*?

m = _____ *n* = _____

c) In terms of the memory map, the ROM memory is to occupy the address space with the lowest address of 0x00000000. What is the highest address in the memory map that the ROM memory occupies in the memory map? Give your answer in the form of eight (8) hexadecimal digits. (Note: assume a byte-addressable memory is being designed.)

Highest ROM address = _____

d) In terms of the memory map, the SRAM memory is to occupy the address space with the lowest address of 0xA0000000. What is the highest address in the memory map that the SRAM memory occupies in the memory map? Give your answer in the form of eight (8) hexadecimal digits. (Note: assume a byte-addressable memory is being designed.)

Highest SRAM address = _____

e) If this memory system is to support an ARM processor with a 32-bit address bus and a 32-bit bidirectional data bus, use the appropriate ARM processor signals and design a circuit that will be connected to the !oe inputs of the ROM memory chips. Your answer should be in the form of a digital logic combinational circuit. (Note: this is a portion of the circuitry that is inside the box labeled 'control' on slide 26 of the notes and produces the !ROMoe signal.)

f) On slide 26, the control circuit generates four (4) write enable signals for the four SRAM chips used in the example (!RAMwe0, !RAMwe1, !RAMwe2, !RAMwe3). How many !RAMwe signals will the control unit need to generate for the memory system you are designing?

# of RAMwe signals = _____

g) For each !RAMwe signal you identified above, give the corresponding circuit that uses appropriate inputs from the ARM processor. Each !RAMwe signal will be an output of a logic gate diagram and is inside the box labeled 'control' on slide 26.

h) Combine all of the logic circuits above into a single diagram that represents the entire circuit in the box labeled 'control' on slide 26. (Note: slide 32 is the similar type of circuit asked for here but that corresponds to slide 26).

2. The AMBA bus supports pipelined accesses meaning that a new access can be initiated before the previous one is finished. Describe how this is possible for the AMBA bus.

3. Is it possible for a system using the AMBA bus to access a memory bank or an I/O device that has a response time slower than the HCLK clock cycle? If not, explain why using the appropriate AMBA bus signals in your response. If yes, explain why using the appropriate AMBA bus signals in your response.

4. The AMBA standard contains specifications for the AHB and the APB bus. The APB bus is intended for use with lower bandwidth peripherals. Why would an embedded system designer choose to use APB instead of AHB, that is what is the advantage offered by using APB? (Note: an incorrect answer is 'because the peripheral is low bandwidth,' you need to tell me why APB is advantageous compared to AHB for low bandwidth peripherals).

5. Why does the I2C bus require pull-up resistors on the SDA and SCL lines?

6. Why does the I2C bus require all devices to connect to it with open-collector drivers?

7. When the I^2C bus is operating in standard mode and the attached devices all have high rail voltages of V_{DD}=3.3V, answer the following, give the following values. (Note: you will have to refer to the I^2C specification that is linked to the class syllabus)

Minimum Low-level Input Voltage = _____
Maximum Low-level Input Voltage = _____
Minimum High-level Input Voltage = _____
Maximum High-level Input Voltage = _____

8. The following voltages are present on the D+ and D- lines of a USB 2.0 bus operating in full bandwidth mode. Give the bitstream that is being transmitted on the bus.

time	t1	t2	t3	t4	t5	t6	t7	t8	t9	t10
D+	3.6	3.6	0.3	3.6	3.6	3.6	0.3	3.6	0.3	0.3
D-	0.3	0.3	3.6	0.3	0.3	0.3	3.6	0.3	3.6	3.6