Redundant signed binary addition based digital-to-frequency converter

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An accumulator-based digital-to-frequency (DFC) converter employing redundant signed binary addition (RSBA) is presented. RSBA is advantageous in that no carry propagation occurs resulting in constant delay regardless of operand word size. Utilising RSBA in the proposed DFC resolves the performance bottleneck in the DFC's conventional implementation and achieves extremely high frequency resolution. In addition, a new RSBA-based 8 : 1 multiplexer is introduced for a complete RSBA implementation of the DFC. Experimental results show an increase of more than 3.5 times in the speed of the accumulator compared to the conventional implementation regardless of bit size of the adder.

Introduction: The flying-adder (FA)-based frequency synthesiser can be viewed as a digital-to-frequency converter (DFC) for on-chip digital controllable frequency synthesis [1]. Owing to its wide frequency range, instant response, and easy integration, the FA-DFC has been widely used in system-on-chip applications [2]. The FA-DFC consists of two units, a simple integer-N PLL providing the reference signals, and the digital processing unit (mainly adder, multiplexer and D-flip-flop), capable of synthesising a wide range of frequencies instantaneously. As its name states, the core of the FA-DFC is the function of addition which generates the control signals for the multiplexer in the FA-DFC to construct the final clock output. This addition operation is crucial for the creation of the output frequency, in that it determines the frequency resolution as well as the highest frequency synthesisable using this architecture [3]. High resolution in the FA-DFC clock output requires a large number of bits in the fractional part of the frequency control word. As a result, the adder/accumulator becomes the bottleneck of the FA-DFC because the higher the frequency resolution, the larger the adder/accumulator is required and hence an increased propagation delay results in the adder circuit due to carry propagation.

We employ RSBA to overcome such a performance bottleneck because no carry propagation occurs in RSBA, which yields constant delay regardless of operand word size. In conventional binary addition circuits using the digit set {0, 1}, there have been many published methods of reducing the delay of large adders by manipulating the way a carry-ripple is propagated and minimising its occurrence as described in [4–6]. One can conjecture that minimising/eliminating the carry-ripple digit propagation would also in fact minimise/eliminate the respective contributing delay, resulting in faster adders. As discussed in [7], redundant signed digit number systems can be used to implement fast addition circuits by taking advantage of the redundancy in the system. In RSBA arithmetic, a normal single binary bit is represented by two bits. For example, the binary number '1' can be represented by '10' (where the first digit is called the sign bit S and the second digit is the magnitude bit M). A radix-2 system is still used, however the digits $\{-1, 0, 1\}$ are incorporated into the system and denoted by $\{\bar{1}, 0, 1\}$. The work described here utilises the addition table defined in Table 1. $\{\bar{1}, 0, 1\}$ is encoded as {00, 01, 10} for implementation (where the string 11 is not used). Since three digits are used in a radix-2 system, redundancy will occur and certain binary strings are able to be represented in more than one way. This redundancy can be used to create addition circuits that do not experience carry ripples. This Letter focuses on incorporating an addition circuit based on the RSBA methodology into the FA-DFC to resolve the speed bottleneck of the adder and achieve a higher frequency resolution.

Table 1: Signed binary addition table with borrow used to translate FA-DFC into RSBA system [7]

$w_i + x_i$	b_{i+1}	b_i	z_{i+1}	y_i
$\bar{1}+\bar{1}$	$\bar{1}$	$\bar{1}$	0	$\bar{1}$
$\bar{1}+\bar{1}$	$\bar{1}$	0	0	0
$\bar{1}+0$	$\bar{1}$	$\bar{1}$	0	0
$\bar{1}+0$	$\bar{1}$	0	1	$\bar{1}$
$0+0$	0	$\bar{1}$	0	$\bar{1}$
$0+0$	0	0	0	0
$1+\bar{1}$	$\bar{1}$	$\bar{1}$	1	$\bar{1}$
$1+\bar{1}$	$\bar{1}$	0	1	0
$1+0$	0	$\bar{1}$	0	0
$1+0$	0	0	1	$\bar{1}$
$1+1$	0	$\bar{1}$	1	$\bar{1}$
$1+1$	0	0	1	0

RSBA multiplexer: Although using RSBA produces fast adders, the caveat to utilising RSBA is that the number system should be kept consistent throughout the design. Otherwise, converting from RSBA back to normal binary involves carry ripples in conversion arithmetic. To solve this problem, we designed a new RSBA-based multiplexer (an 8:1 one for the FA-DFC) for use with the adder as shown in Fig. 1. The RSBA multiplexer consists of control logic and a tree of logic gates. While a standard 2:1 multiplexer requires one select line, an RSBA-based 2:1 multiplexer requires two select lines (SEL_S for the sign bit and SEL_M for the magnitude bit). Likewise, for an RSBA 8:1 multiplexer, six select lines in total are required, three for SEL_S and three for SEL_M. The role of the control logic is to select the appropriate output path. When one path is selected, the control logic outputs a logical '1' to enable the respective AND gate. The tree of OR gates that follow propagate the signal to the output. The control logic is composed of a table of values that maps the select lines to an appropriate output path selection.

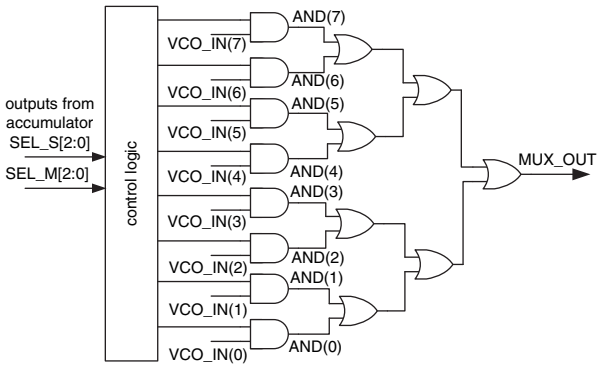

Fig. 1 *Theoretical RSBA 8:1 multiplexer*

RSBA flying adder: The FA-DFC with the new adder/accumulator and multiplexer is described and validated utilising HDL functional simulations. Utilising the method in [7], the adder/accumulator inside the FA-DFC was synthesised to an RSBA system. The conventional 8:1 multiplexers were replaced with the new RSBA-based 8:1 multiplexers. Fig. 2 depicts the complete FA-DFC architecture using the RSBA addition circuit.

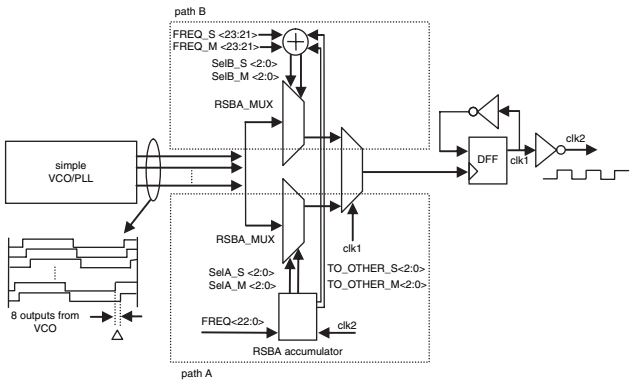

Fig. 2 *Flying-adder using RSBA system*

Experimental results: A conventional and RSBA-based adder/accumulator are synthesised using a standard cell library from IBM 0.13 μm (CMRF8SF) process and the results reported from the Synopsys® Design Compiler® tool on the two designs are compared. We report in Tables 2 and 3 the performance, area and power consumption for various word sizes for the adder/accumulator block. The area was taken using the area of a standard 1X drive strength NAND2 gate. In Table 4, we compare the report on the critical path, area and power consumption of a conventional 8:1 multiplexer and the new RSBA 8:1 multiplexer.

Table 2: Conventional adder/accumulator used in flying adder (multiple bit size synthesised performance results as reported from Design Compiler)

	Conventional adder/accumulator FA		
Adder size	Speed (ns)	Area (units of NAND2)	Dynamic power consumption (mW)
24-bit	0.81	517.25(324.25192.99)	4.2842(3.6496,0.6346)
32-bit	0.83	636.75(444.50,192.25)	4.6412(3.8652,0.776)
48-bit	1.1	1227.75(870.00,357.75)	6.4727(5.3746,1.0981)

Table 3: New RSBA adder/accumulator used in flying adder (multiple bit size synthesised performance results as reported from Design Compiler)

	New RSBA-based adder/accumulator FA		
Adder size	Speed (ns)	Area (units of NAND2)	Dynamic power consumption (mW)
24-bit	0.22	1047.50(518.50,528.99)	15.9265(13.7137,2.128)
32-bit	0.22	1978.25(1257.25,720.99)	25.8423(20.593,5.2496)
48-bit	0.22	2897.743(1905.75,991.99)	32.6018(24.7033,7.8985)

Table 4: Standard multiplexer against RSBA-based multiplexer

	8:1 multiplexer comparison		
Type	Critical path limit (ns)	Area (units of NAND2)	Dynamic power consumption (uW)
Conventional	0.52	12.5(72,0)	8.1187(5.4736,2.6450)
RSBA	0.50	59.5(37.5,22)	28.1325(18.7376,9.9349)

Synthesised results show that in the RSBA adder/accumulator we obtain constant speed regardless of the word size as expected due to the properties of RSBA. By contrast, for the conventional adder, as word size increases, speed decreases and area and power consumption increase. Specifically for a 24-bit adder, the RSBA has a 3.7 times performance improvement over the conventional one. Even if we account for 100% wire and routing delay, we still see almost a 2.0 times improvement in performance. The improved performance does come with increase in area (two times) and power dissipation (3.5 times). However, experimental results show that the total power dissipation of the adder only accounts for ($<10\%$) of that of the DFC. This means replacing the conventional adder in the DFC with an RSBA-based results in an increase of only 25% of the total power consumption of the DFC. Therefore the increase in power is justified when a higher frequency resolution is desired. Note the power consumption reported by Synopsys® assumes 100% activity, which in practice will be much lower. This is confirmed by circuit-level Cadence simulation results: 1.2 mA for the accumulator and 13 mA for the complete DFC. The increase in area is less of a concern for deep sub-micron or nanometre technology as the device sizes become smaller.

In addition, the increase in area and power consumption in the RSBA multiplexer is negligible because the total power dissipation of the multiplexer only accounts for a small fraction of the total power dissipation of the synthesiser ($<1\%$).

Conclusion: This Letter introduces an RSBA based adder/accumulator in the FA-DFC that resolves the performance bottleneck caused by the adder. A new RSBA multiplexer is presented to allow for the full integration of the RSBA adder into the FA-DFC. The RSBA adder demonstrates superior speed performance regardless of the bit/word size, thus a very fine frequency resolution is achieved in the frequency synthesiser.

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