Call for Papers

52nd IEEE International Symposium on Multiple-Valued Logic

ISMVL 2022

The Multiple-Valued Logic Technical Committee of the IEEE Computer Society will hold its 52nd annual symposium in **Virtual mode** on May 18-20, 2022. You are invited to submit original papers, surveys, or tutorial papers on any subject in the area of multiple-valued logic, including but not limited to:

Algebra and Formal Aspects	Logic Design and Switching Theory
Automatic Reasoning	Test and Verification
Logic Programming	Spectral Techniques
Philosophical Aspects of MVL	Circuit/Device Implementation
Fuzzy Logic and Soft Computing	VLSI Architecture and Computing
Data Mining	System-on-Chip Technology
Machine Learning	MVL in Nanotechnology
Quantum Informatics	MVL in Medical Technologies
Reversible Computing	MVL in Data Science and Analytics
MVL aspects of Autonomous Systems	MVL in Computer Security

Authors should submit papers through the [Easychair website](#) as PDF files following the IEEE style guidelines for conference proceedings. Each manuscript should include a 50-100 word abstract and be 6 pages in length. Up to 2 additional pages may be included with extra page charges of $100 per page. All accepted papers will be published by IEEE and appear in IEEEXplore. More information can be found at [ISMVL 2022 website](#).

   In conjunction with the conference, the international Workshop on Post-Binary ULSI Systems (ULSIWS) will be held on May 18, 2022. A separate call for papers for ULSIWS is available at the [ULSIWS website](#).

Paper Submission :
~~November 1, 2021~~
~~December 1, 2021~~
December 17, 2021
Author Notification:
January 28, 2022
Camera-Ready Version:
February 25, 2022
ISMVL Symposium:
May 18-20, 2022
ULSI Workshop:
May 18, 2022 (morning)

For questions, please contact:

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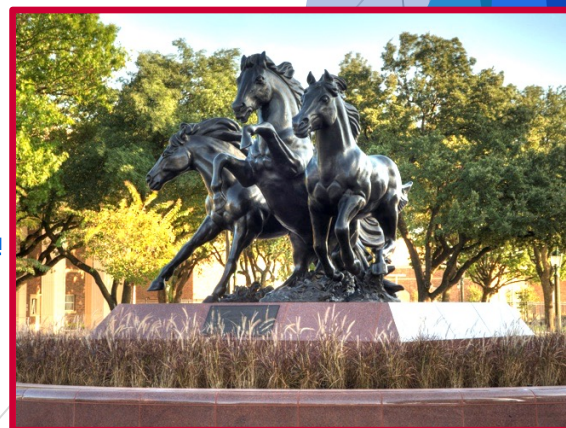mitch@smu.edu

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