A Novel

Flying-Adder-Digital-to-Frequency-Converter-Based Large-\(N\) Frequency Multiplier

Wickham Chen, Student Member, IEEE, Ping Gui, Member, IEEE, Liming Xiu, Senior Member, IEEE

Abstract—In video and graphic applications, synthesizing a high-frequency clock from a very low-frequency clock is often needed. In these applications, the multiplication ratio \(N\) can be very large (on an order a thousand or greater). Due to many implementation difficulties, it is a nontrivial task for a conventional Phase-Locked Loop (PLL) to handle such a large \(N\). This paper presents a novel approach for frequency multiplication that is able to handle such a large \(N\). This approach employs minimum analog complexity and maintains high performance. Additionally, a random dithering technique is introduced in this architecture to reduce spurious noise in the clock output. Random dithering can also be used for reshaping the clock spectrum for lower electromagnetic interference (EMI).

Index Terms—Frequency Multiplier, Flying-Adder (FA), Frequency Synthesis, Phase-Locked Loop (PLL), Digital-to-Frequency Converter (DFC), Random Dithering, Spread Spectrum Clock Generation (SSCG), Electromagnetic Interference (EMI).

I. INTRODUCTION

In video decoding and graphics digitizing processes often require constructing a high-frequency pixel clock from a very low-frequency clock to accommodate various resolutions and refresh rates[1]. In these applications, the input frequency typically ranges from Hz to KiloHz (KHz); the multiplication ratio \(N\) can be very large (\(N > 1000\)). Conventional integer- \(N\) Phase-Locked Loop (PLL) is commonly used for frequency multiplication [2]-[5]. However when \(N\) is large this approach becomes unfeasible. First, when \(N\) is large, the output clock frequency can drift since the oscillator only updates infrequently. Second, the noise level or jitter associated with the low-frequency input is typically high, which could potentially be coupled to the output clock through the loop. Moreover as \(N\) increases, the magnitudes of all the voltage-controlled-oscillator (VCO)-extrinsic noises (including reference jitter, reference feed-through, charge pump noise and divider jitter) aggravate by a factor of \(N^2\) on the PLL output [6]. Third, a low-frequency reference clock in the PLL requires a low loop bandwidth. This can result in very large loop filter components (capacitors and resistors) which cannot be easily integrated on chip.

Reference [5] describes a self-biased Integer-\(N\) PLL based frequency synthesizer with constant loop dynamics independent of \(N\). However, the design is analog intensive and the implementation cost is high. Moreover, this design is not able to address the challenge when the input reference frequency is very low (in Hz to KHz range).

There have also been developments using Delay-Locked Loop (DLL)-based approaches to implement frequency multiplication [7]-[9]. A good example is in [7]. The main advantage of using a DLL comes from the fact that the jitter inside the DLL loop does not accumulate. Also, a DLL is a first-order feedback system, thus it is inherently stable. A multiplying DLL (MDLL) combines the frequency multiplication capabilities of a PLL with the low phase noise characteristics of a DLL. However, using a MDLL such as the technique shown in [7] has some drawbacks. The most severe one is the lost of oscillation when there is a missing edge at the reference clock. Since there is no filter function in the loop for attenuation, the input reference will be directly fed to the output as frequency spurs in the spectrum. Although this MDLL frequency multiplication method is useful for some applications, its usage is limited especially when the multiplication factor is large. In these cases, the reference clock only comes in infrequently thus the ring oscillator inside the MDLL accumulates significant jitter proportional to the multiplication factor (negating the purpose of using a DLL).

This paper presents a novel frequency multiplier that can handle a large \(N\) which utilizes components of a digital-to-frequency converter (DFC) and a frequency-to-digital converter (FDC). Fig. 1 depicts the high-level view of the proposed system architecture. By employing both a DFC and a FDC, frequencies are represented in the digital or software domain. Digital or software processing can be utilized to produce the desired relationship: \(f_{out} = N \cdot f_{in}\). It is noted that the \(N\) in the figure does not have to be an integer; any real number can be used.

\[
\begin{array}{c}
f_{in} \xrightarrow{DFC} Digital \text{ Value} \\
Digital \text{ or Software Processing} \\
\xrightarrow{DFC} Digital \text{ Value} \\
\xrightarrow{FDC} f_{out}
\end{array}
\]

\[f_{out} = N \cdot f_{in}\]

Fig. 1. The overall system architecture.

A Flying-Adder-based Digital-to-Frequency Converter (FA-DFC) is employed in the proposed architecture. The FA-DFC synthesizer is based on the concept of Time-Average-Frequency [10]. It has two useful features: arbitrary frequency generation and a seamless instant frequency switch, shown in Fig. 2. These two features grant many system-level advantages to electronic system designers. The

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W. Chen and P. Gui is with Southern Methodist University Dallas, TX 75205 USA (e-mail: wickham@lyle.smu.edu, pgui@lyle.smu.edu).
L. Xiu (e-mail: lmxg96@gmail.com).
counterpart of a DFC. FDC, can be realized in many ways, such as using a digital counter driven by a known high frequency clock, or using a Time-to-Digital converter [11]-[14].

![Fig. 2. The Flying-Adder DFC’s arbitrary frequency generation and instantaneous frequency response.](image)

The concept presented in Fig. 2 is able to solve the problems associated with the analog PLL when dealing with a large N multiplication. First, this architecture electrically decouples the generated output clock from the very noisy low-frequency input clock. Thus, the large jitter from the input will not propagate to the output. Second, this design eliminates the low loop bandwidth constraint imposed by the low-frequency input. Third, the final output of this multiplier exhibits an instant response to a change in N or a change in the input frequency. This instant response characteristic is achieved by employing the FA-DFC. Fourth, N can be very large (the input clock can be a very low frequency, such as in Hz range); and N does not have to be an integer, but can be a real number.

In addition, a random dithering technique can be employed to manipulate the output frequency spectrum for the reduction of spurious component or the spreading of the clock energy.

This paper is organized as follows. Section II presents the proposed FA-DFC based frequency multiplier architecture and the comprising circuit building blocks. Section III describes the proposed random dithering method and circuitry. Section IV shows the experimental results, and Section V draws the conclusion.

## II. THE FA-DFC-BASED FREQUENCY MULTIPLIER

### A. Overall System Architecture

![Fig. 3. The block diagram of the FA-DFC-based frequency multiplier.](image)

Fig. 3 is the circuit block diagram of the proposed design which implements the architecture shown in Fig. 1. This design is capable of handling a large N frequency multiplication. ClkIn is the input clock with an unknown frequency typically in the KHz or Hz range. A fixed-frequency PLL, which is locked to a clean reference signal ClkRef, is used for generating the multiple clock signals with frequency $f_1$ at the VCO for FA-DFC. One of the PLL/VCO outputs, ClkHi, is used to drive the Frequency-Measurement block which measures the frequency of the input clock ClkIn. Since ClkHi is a high-frequency signal typically in the range of GHz, a counter can be used effectively in the frequency measurement block to measure the frequency of ClkIn into digital value with high precision. This counter can be viewed as one type of DFC. Both the frequency measurement output and the intended multiplication ratio N are fed into the Control-Word-Conversion block, which calculates the final control word FREQ. The resulting FREQ, also in digital format, is sent to the control port of the FA-DFC. Based on FREQ, the FA-DFC generates the output clock ClkOut of frequency $f_2$ with the established relationship $f_2 = N \cdot f_{in}$. A post divider M shown in Fig. 3 is inserted on the output to expand the frequency range. A dithering function is applied to reshape the spectrum of the output clock. Except for a fixed-frequency PLL, all other components in this architecture are digital.

In the following subsections, each component will be described in detail.

### B. Flying-Adder Digital-to-Frequency Converters (FA-DFC)

The key component in the proposed frequency multiplication architecture is the Flying-Adder based DFC (FA-DFC) [15, 16]. The detailed circuit implementation can be found in [17] and the theoretical foundation is established in [10]. The two unique features of the FA-DFC are arbitrary frequency generation and instantaneous frequency switching. Since the FA-DFC is used in the proposed frequency multiplier, these features are also commutative to the frequency multiplier.

![Fig. 4. The principal working mechanism of FA-DFC.](image)

Fig. 4 depicts the principal working mechanism of FA-DFC. FA-DFC mainly consists of two parts: 1) a very basic fixed-frequency PLL with a multiple-stage VCO to provide multiple clock with the same frequency but evenly distributed phases, and 2) digital circuits, mainly an adder, a multiplexer...
and a DFF, to generate the final clock output based on the control word FREQ. The adjacent VCO output signals differ in phase by $\Delta$, 

$$\Delta = \frac{T_{\text{VCO}}}{K},$$

(1)

where $T_{\text{VCO}}$ is the period of the VCO clock and $K$ is the number of VCO output phases ($K=8$ in our implementation as 4 differential delay stages are used). The desired period $T_{\text{out}}$ (or frequency) of FA-DFC output is then [17]

$$T_{\text{out}} = 1/f_{\text{out}} = \text{FREQ} \cdot \Delta.$$  

(2)

The multiple-stage VCO can be viewed as a phase divider, which expands the operating range of the FA-DFC to:

$$\left(\frac{1}{8}\right)f_{\text{VCO}} \leq f_{\text{out}} \leq \left(\frac{7}{8}\right)f_{\text{VCO}}.$$  

(3)

Depending on FREQ, the FA-DFC has two modes of operation: integer and fractional mode. FREQ can be expressed as

$$\text{FREQ} = I + r,$$  

(4)

where $I$ is the integer part and $r$ is the fractional part. In the integer mode where $\text{FREQ} = I$, the increment in the address bits for the multiplexer is a constant value, thus the synthesized clock output has an uniform period given by $T_S = I \cdot \Delta$. In the fractional mode, $\text{FREQ} = I + r$ is a real number and the FA-DFC operates according to the concept of time average frequency. In other words in the time domain instead of consisting only one type of clock cycle, there are two types of cycles, $T_S$ and $T_L$, with $T_S = I \cdot \Delta$, and $T_L = (I + 1) \cdot \Delta$. The frequency of the occurrence of $T_L$ is determined by $r$ in FREQ. The average period (or frequency) of these cycles over a period of time is the desired period (frequency) of the output clock.

C. Frequency Measurement (DFC) and Information Conversion

The Frequency-Measurement block in Fig. 3 is used to detect the frequency of the input clock ClkIn and convert it into a digital value. In this design, the DFC is implemented as a simple counter driven by ClkHi of frequency $f_1$. The DFC’s output is fed to the conversion block which multiplies the result with the desired multiplication factor $N$ and converts it into the frequency control word (FREQ) for the FA-DFC.

From the frequency measurement, we have:

$$\frac{1}{f_i} = X \cdot \frac{1}{f_1},$$

(5)

where $X$ is the counter output, a digital value and $f_1$ is the frequency of ClkHi. For a final clock output $f_{\text{out}}$, which is $N$ times the frequency of ClkIn, the following is true:

$$f_{\text{out}} = \frac{f_2}{M} = N \cdot f_{\text{in}},$$

(6)

Combining (2), (5) and (6) yields FREQ as:

$$\text{FREQ} = \frac{\tau_1 X}{N \cdot M \cdot \Delta}.$$  

(7)

In our design, we utilize a 1 GHz VCO output and a four-stage VCO. Thus we have:

$$\text{FREQ} = \frac{8 \cdot X}{M \cdot N}.$$  

(8)

For example, suppose we need to multiply a slow input clock ClkIn by $N=2000$, to create a high-frequency pixel clock ClkOut. Assuming ClkIn has a frequency of 80 KHz, then the DFC, driven by a 1 GHz clock, gives a count of $X=12,500$. Based on (8) and assuming $M=4$, the required FREQ is computed as

$$\text{FREQ} = \frac{8 \cdot X}{M \cdot N} = \frac{8 \cdot 12500}{4 \cdot 2000} = 12.5$$

(9)

D. Reference Generation

The FA-DFC is based on a group of equally-spaced reference signals. These signals are generated from a fixed-frequency VCO which is locked to a clean reference through PLL. The structure of this reference generator is shown in Fig. 5. The input reference is a clean 25 MHz signal. The divider used inside the loop has a ratio of 40 and the VCO is targeted at 1 GHz. The loop bandwidth is designed around 1 MHz.

Fig. 5. PLL used for reference frequency generation.

As shown in Fig. 6, the VCO is constructed with four delay stages in ring style with each stage consisting of two cross coupled NAND gates. Eight single-ended outputs are generated from this VCO. The supply of the VCO (Vtune) is generated from an operational amplifier (OpAmp). This OpAmp controls the VCO’s oscillation frequency. This PLL/VCO structure has certain advantages: a) Using the OpAmp output as the supply of the VCO can effectively isolate the VCO from the power supply noise. b) The VCO is constructed in differential fashion which can further reduce the noise level. c) The VCO does not have any start-up problem which is very important in commercial usage.

Fig. 6. The VCO made of four stage cross-coupled NAND gates.
III. RANDOM DITHERING FOR MANIPULATING OUTPUT SPECTRUM AND GENERATING SPREAD SPECTRUM CLOCK

A. Random Dithering for manipulating output spectrum

The fractional bits in FREQ produce prolonged cycles with a period of \( T_f = (1 + 1) \cdot \Delta \). These cycles appear periodically in the FA-DFC output and as a result create spectral spurs in the frequency domain [10]. In certain applications, such as when the FA-DFC clock is used to drive sampling systems, these spurs are unfavorable to system performance if they are close to the central carrier frequency. Dithering techniques can be employed to break up the periodical patterns in the clock waveform so that the effects of the spurs are diminished [10]. In this paper, a random dithering technique is designed and implemented to reduce the fractional spurs. The same technique can be also used to shape the clock frequency spectrum.

Random dithering breaks up the periodicity embedded in the accumulator's overflow generation pattern by adding random noise to FREQ. There are two parameters to control the dithering function: the rate (Dth_Clk) of random dithering and the magnitude (Dth_Mag) of the random noise. These two control mechanisms can be readily implemented in the existing FA-DFC architecture.

Our simulations show that a dithering rate proportional to the magnitude of the FREQ's fractional part, \( r \), results in maximum dithering effectiveness. When \( r \) is large (\( 0.1 < r < 0.9 \)), the pro-longed cycle \( T_f \) occurs more often than in the case when \( r \) is small (\( 0.01 < r < 0.09 \)), a faster Dth_Clk produces a more effective dithering result. Likewise, when \( r \) is small a slower Dth_Clk produces the more effective dithering result. In our design, Dth_Clk is supplied by the fixed-frequency PLL combined with a programmable divider which allows for various dithering rates to be implemented.

In addition, it is also found that it is most effective to have the magnitude of the applied noise proportional to the size of the FREQ's fractional part. For example, for \( 0.1 \leq r \leq 0.99 \), simulation results have shown that a Dth_Mag value of approximately 0.1 suffices. Likewise, for \( 0.01 \leq r \leq 0.099 \), a Dth_Mag value of approximately 0.01 is adequate. Dth_Mag is supplied by a linear feedback shift register (LFSR)-based random number generator. Depending on the desired Dth_Mag, the corresponding binary representation is used to select the appropriate bits which are added to the fractional part of FREQ.

The random noise can be generated by using the random number generator which can be realized in digital domain. There have been many published mathematical methods of generating random numbers [19] [20]. An LFSR approach is taken due to the fact that no arithmetic circuits have to be built and its ease of implementation. Fig. 7 shows the schematic of the dithering block used in our design. The random noise added needs to be of zero mean; otherwise FREQ will change, causing deviation from desired output frequency. To accommodate this effect, the mean value of the LFSR-generated random numbers must first be subtracted from the control word.

Fig. 8 and Fig. 9 are the SPICE simulation result where the dithering effect can be observed. Fig. 8 depicts a scenario where \( FREQ = 10.01, Dth_Clk \) is 1/16 of the PLL/VCO clock frequency, and Dth_Mag is approximately 0.01. We find that the majority of the spurs are no longer visible and the magnitude of the spurs close to the central frequency is now reduced. Fig. 9 depicts a case where \( FREQ = 10.1, Dth_Clk \) is equivalent to the PLL/VCO clock frequency, and Dth_Mag is approximately 0.1. Here spurs are also removed on the spectrum after dithering is applied.

B. Random dithering for spread spectrum

In certain applications, the Electromagnetic Interference (EMI) is a serious design concern. Spread Spectrum Clock Generation (SSCG) technique can be used to spread the highly concentrated clock energy to a boarder band so that EMI is low enough to pass specified regulations. The majority of the existing SSCG approaches use the method of applying a modulation profile at the divider inside the PLL loop [21]-[23], which is analog intensive and hard to control precisely. Reference [23] uses the multiple taps generated from a digital delay line to construct the SSCG which can be considered a subset of FA-DFC SSCG approach introduced in [10]. In our design, the SSCG function is achieved by using the same random dithering method discussed in section III.A.

Fig. 10 shows the spread spectrum effect. In this case we use a large magnitude of dithering to reshape the spectrum so that the overall EMI is reduced. In Fig. 10 we see that \( FREQ = 10.1, Dth_Clk \) of 1/16 of the output clock frequency, and a noise magnitude Dth_Mag of approximately 0.3 is used. Here we observe a reduction of about -16 dB in the carrier energy and that the energy is spread in a large frequency range around 250 MHz.
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IV. EXPERIMENTAL RESULTS

The system described in Fig. 3 is manufactured in 0.13μm IBM CMRF8SF technology. Fig. 11 shows the layout of the design and the micrograph of the actual chip. The fixed-frequency PLL and the FA-DFC are designed by the custom mixed-signal design approach. All the rest of the blocks are constructed in digital design flow through Hardware Description Language (HDL) design capture, logic synthesis and place & route. The VCO has eight outputs. The frequency control word \( FREQ \) of FA-DFC is configured as 24 bits [23:0] (3 bytes for easy programming). The top four most significant bits, \( FREQ \) [23:20], are used for integer part whereas the \( FREQ \) [19:0] is reserved for fractional part. The total chip area is 1300 μm x 1800 μm (include the IO ring and bond pads). The area used by the reference PLL is 520 μm by 325 μm. The FA-DFC uses only 190 μm by 135 μm.

Fig. 11. The layout and micrograph of chip.

Fig. 12 depicts the test environment used to evaluate our system. A Tektronix AFG3251 waveform generator provides the clean reference (ClkRef) for the fixed-frequency PLL. The Agilent 33250A function generator provides the input clock signal ClkIn (KHz or below). The Tektronix TDS7404 Digital Oscilloscope is used to capture the output clock waveform. The HP 8495E spectrum analyzer is used to study the output spectrum. A Spartan 3 FPGA provides the control signals for the loop structure. A PC, with LabView™ capability, controls the whole test environment.

Fig. 12. The test environment.
A. Jitter measurement

As shown in Fig. 3, the PLL provides the reference signals for the following FA-DFC. The quality of these reference signals is critical for the performance of our system. Fig. 13 is the jitter measurement when the PLL output frequency is 1 GHz. Its RMS jitter is measured to be around 6.7245 ps. This measurement result is pessimistic since the observed output has passed through the post divider, several buffers and the single-ended output IO cell. The signals inside the VCO, which are differential, could have a better quality. Also, a better reference source such as a crystal could result in smaller jitter number.

![Fig. 13. The jitter measurement result of VCO output at 1 GHz.](image)

<table>
<thead>
<tr>
<th>Clock Period (ps)</th>
<th>Clock Jitter (ps)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mean</td>
<td>6.7245</td>
</tr>
<tr>
<td>Max</td>
<td>10.0275</td>
</tr>
<tr>
<td>Min</td>
<td>0.9778</td>
</tr>
<tr>
<td>Peak</td>
<td>49.9211</td>
</tr>
<tr>
<td>Std Dev</td>
<td>6.2256</td>
</tr>
<tr>
<td>Population</td>
<td>103.30</td>
</tr>
</tbody>
</table>

![TABLE I NOISE ISOLATION IN THE LOOP STRUCTURE](image)

B. Loop functionality verification

The goal of this architecture is to multiply a low frequency input in KHz or even Hz range to several hundred MHz. This has been verified by many run of tests in our evaluation of the chip. During these tests, the input frequency is set and the multiplication factor is swept. Fig. 14 is the result of one of the many test runs where the input clock was set to 250 kHz and \( N \) was swept from 500 to 2000. It shows that the system achieves the correct multiplication as expected.

![Fig. 14. Measured Functional Results with input reference of 250 kHz.](image)

C. Instantaneous response of FA-DFC

Instantaneous response is a key feature of the FA-DFC operation [16] where the new frequency is readily available the next cycle after FREQ is updated. Compared to tradition PLLs which require certain settling time before locking to a new frequency, this is a very desirable feature for system level design because the circuits can transit seamlessly from one frequency to another. To take advantage of the instantaneous response of the FA-DFC in the proposed frequency multiplier, the conversion block does not update FREQ until it has a new value ready. Fig. 15 is the test result which shows this characteristic. In this plot, the slow clock changes from 400 kHz to 200 kHz and the \( N \) ratio is at 1000. As can be seen, the output clock follows it seamlessly from 400 MHz to 200 MHz. The plot is measured from the Tektronix TDS7404 oscilloscope.

![Fig. 15. Instantaneous switching characteristic.](image)

Fig. 16 is another demonstration of this instantaneous frequency response characteristic. In this plot, the bottom waveform represents a control signal which switches the input slow clock from 250 KHz to 400 KHz. The \( N \) ratio is set at 1000. As can be seen, the output clock follows it seamlessly from 250 MHz to 400 MHz. The data log is measured with LabView™.
Fig. 16. Instantaneous switching characteristic.

D. Random dithering to reshape output spectrum

Fig. 17 and 18 illustrates this system’s capability to reshape the output spectrum. The data was obtained from an Agilent 8495E Spectrum Analyzer and then sampled via GPIB through Labview®. These results have confirmed the behavioral and circuit-level simulations. In Fig. 17, $N = 1140$ and $ClkIn$ is 250 kHz, thus the expected output frequency is $N \cdot ClkIn = 1140 \cdot 250$ kHz $= 285$ MHz. In this case, $FREQ = 7.01$, $Dth_Clk$ is 1/16 of the PLL/VCO clock frequency, and $Dth_Mag$ is approximately 0.01. As a result of dithering, a spur free output spectrum is seen in the lower graph of Fig. 17.

In Fig. 18, $N = 1278$ and $ClkIn$ is 250 kHz, thus the expected output frequency is $N \cdot ClkIn = 1278 \cdot 250$ kHz $= 319.5$ MHz. In this case $FREQ = 6.25$, $Dth_Clk$ is 1/64 of the PLL/VCO clock frequency, and $Dth_Mag$ is approximately 0.1. The lower graph of Fig. 18 shows the effective dithering result.

E. Random dithering for spread spectrum

In Fig. 19, we demonstrate the spread spectrum capability. Here $N = 1000$ and $ClkIn$ is 250 kHz, thus the expected output frequency is $N \cdot ClkIn = 1000 \cdot 250$ kHz $= 250$ MHz. The original center frequency of 250 MHz is now spread across a span of approximately 10 MHz. Here $FREQ = 8$, $Dth_Clk$ is 1/64 of the PLL/VCO clock frequency, and $Dth_Mag$ is approximately 0.3. The lower graph of Fig. 19 shows the spread effect.
V. CONCLUSION

We have presented a novel frequency multiplier which can multiply a low-frequency, noisy clock into a high-frequency output with very low jitter. Silicon measurement results have demonstrated the following features of this technique: 1) the input clock frequency can be very low, even in Hz range, and the multiplication ratio N can be very large, on an order of thousand greater; 2) the noise associated with the input will not propagate to the output; 3) the output clock can follow instantly with the change in input clock frequency or the multiplication ratio; 4) dithering circuits are shown capable of spreading the clock spectrum or reducing the spurious frequencies. This system is useful for many commercial applications, especially for video/graphic/image applications.

REFERENCES