A 2-Gb/s Optical Transceiver With Accelerated Bit-Error-Ratio Test Capability

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***Abstract*—Accelerated bit-error-ratio (BER) measurement techniques using specialized test equipment are widely used for rapidly verifying the low BER ($< 10^{-12}$) of high-performance optical links. However, once these links are deployed in the field, it takes days to weeks to complete such BER measurements using a conventional testing method. This paper describes an optical transceiver architecture with on-chip accelerated BER measurement mechanics that reduces "in the field" BER testing time to minutes. The approach described in this paper uses an integrated interference generator to degrade receiver performance and raise the BER to a range that allows a substantially reduced measurement time. Values of BER versus the amount of interference are then extrapolated to the point of zero artificial degradation for actual BER. A 0.5-μm complementary metal–oxide–semiconductor, 2-Gb/s, four-channel optical transceiver chip was designed, fabricated, and tested to serve as a vehicle for verifying the concept. The experimental results show excellent agreement between the extrapolated and actual BER values. The architecture described here points to a practical built-in self-test capability for optical links within high-performance digital systems, specifically in board- and backplane-level interconnections.**

***Index Terms*—Bit-error ratio (BER), parallel-optical transceiver, vertical-cavity surface-emitting laser (VCSEL).**

I. Introduction

PARALLEL-OPTICAL links are a promising candidate for use within high-speed digital systems, specifically for board-level and backplane interconnect applications [1]–[4]. These systems require optical links that operate at gigabit channel data rates and are essentially free from random errors (e.g., BER $< 10^{-12}$). With such low link BER, conventional measurement techniques, such as counting the errors produced when operating the link at the designed bit rate, become impractical. For example, testing a 2.5-Gb/s link for a BER value of 10^{-12} with 95% confidence, by waiting for 100 bit errors to occur, would take more than 11 h. However, high-speed digital systems need fast, reliable, and inexpensive "in the field" test capability. In certain applications, such as avionics and defense, this test capability is a necessity. In a typical scenario, the system performs a self-test during power-on to identify system components that are not performing to specification. If defective components are found, the system does not activate.

It is well known that the time to test optical link BER can be dramatically reduced using accelerated BER measurement techniques [5], [6]. These techniques are widely used to determine the link sensitivity and BER in fiber-optic transmission systems [7], [8]. They artificially degrade the optical channel in a controlled manner to raise the bit-error rate to a range that requires much less time to measure (e.g., a BER of 10^{-4} to 10^{-10}). The resulting BER measurements are then extrapolated to determine the true BER of the data link being tested. Typically, the optical link is degraded by introducing an artificial interference signal to the optical receiver or by attenuating the transmitted optical signal. Accelerated BER measurement requires a laboratory setup with specialized equipment such as a bit-error-rate tester (BERT) consisting of a pattern generator and an error detection unit. To be effective, this test equipment must be replicated for every channel of the parallel-optical link being measured, which dramatically increases the testing costs for parallel-optical links.

Although accelerated BER measurement methods reduce the time to test optical link BER from days to minutes, they are currently not feasible for "in the field" testing because 1) there are no means of introducing artificial noise into the link and 2) it is impractical to include laboratory test equipment with every link in the system.

This paper describes an optical transceiver architecture that makes "in the field" BER testing possible. The approach consists of an interference generation circuit integrated with the optical receiver combined with on-chip BERT and extrapolation circuits. The interference signal is a random sinusoidal or square waveform having a much lower frequency than the link bit rate. It is introduced at the receiver front end, mimicking either artificial noise current at the photodetector or artificial noise voltage in the receiver threshold level. The BERT circuits consist of a digital pattern generator and error detection subcircuits. The extrapolation circuit computes the actual link BER based on BERT results for the degraded optical link.

A 0.5-μm complementary metal–oxide–semiconductor (CMOS) 2-Gb/s, four-channel optical transceiver chip has been designed, fabricated, and tested to serve as a vehicle for

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verifying the proposed architecture. To reduce design time and risk, digital circuitry for the BERT was implemented using an field-programmable gate array (FPGA) connected to the transceiver, and extrapolation was done manually. An external interference generator was used to allow for maximum flexibility. The transceiver itself includes additional input/output (I/O) ports and interface circuits to facilitate accelerated BER measurement. A free-space optical link system was built to evaluate the accelerated BER measurement techniques. Experimental results show excellent agreement between extrapolated and actual measured BER values. Specifically, accelerated BER testing was performed on an optically attenuated 1.5-Gb/s link to obtain an extrapolated BER of $1.3{*}10^{-11}$ while a 10-h BER measurement shows the actual link BER to be $1.4{*}10^{-11}$. Multiple BER measurements performed with varied optical power showed close correlations between actual BER, extrapolated BER, and predicted BER, assuming the link noise was Gaussian.

To the authors' knowledge, this is the first report of accelerated BER measurement that does not use specialized test equipment and has been successfully correlated to actual link BER. The results point to the feasibility of directly integrating accelerated BER measurement with optical transceiver circuits. This capability is critical to the adoption of optical links in applications where "in the field" testing of system components is a requirement.

The paper is organized as follows. In Section II, the analysis of the BER with Gaussian noise and artificial interference present in the optical channel is described. Section III details the proposed extrapolation technique for ultralow BER measurement. The custom transceiver design and system integration are summarized in Section IV, and the experimental results are presented in Section V.

II. Analysis of Bit-Error Ratio

A. Channel BER With Gaussian Noise

In general, error-causing noise in optical links may include thermal noise, shot noise, reflection-induced noise, laser intensity noise, modal noise, crosstalk, etc. In most cases of practical interest, thermal noise dominates the receiver performance such that the sum of all the noise can be assumed to have a Gaussian distribution. Analysis based on this assumption can yield valid characterization while greatly reducing the computational cost. In some other cases, non-Gaussian noise sources such as modal noise or crosstalk may limit the sensitivity of the system. The later case has recently been the subject of much research focused on modeling, BER floor prediction, simulation techniques, and link power consequences [9]–[13].

For a single-channel, ON–OFF-keyed, intensity-modulated optical link, BER is determined by the signal-to-noise ratio (SNR) at the receiver. In such a system, a typical receiver consists of a photodetector, transimpedance amplifier (TIA), and decision circuitry. The signal at the decision circuit input is proportional to the current input to the TIA. The decision circuit compares the signal to a reference voltage, which is generated by reference threshold current $I_{\rm th}$. An estimate for the error probability $P_{\rm e}$ or BER, with Gaussian approximation, can be described by [14]

$$\begin{aligned} P_{\rm e} &= P(1)P(0|1)+P(0)P(1|0) \\ &= \frac{1}{2}\left[P(1){\rm erfc}\left(\frac{I_1-I_{\rm th}}{\sqrt{2}\sigma_1}\right)+P(0){\rm erfc}\left(\frac{I_{\rm th}-I_0}{\sqrt{2}\sigma_0}\right)\right] \end{aligned} \quad (1)$$

where $P(1)$ and $P(0)$ are the probabilities that a "1" or a "0" is transmitted, while $P(1|0)$ and $P(0|1)$ are the probabilities of receiving a "1" or a "0", given that the other was sent. I_1 and I_0 are the induced photocurrent from the detector, and σ_1 and σ_0 are the root-mean-square (rms) noise of a "1" or a "0" bit. The erfc is the complimentary error function, defined as [15]

$${\rm erfc}\,(x) = \frac{2}{\sqrt{\pi}}\int_x^\infty e^{-u^2}du. \quad (2)$$

Assuming equally likely "1"s and "0"s, (1) can be simplified as

$$P_{\rm e} = \frac{1}{4}\left[{\rm erfc}\left(\frac{I_1-I_{\rm th}}{\sqrt{2}\sigma_1}\right)+{\rm erfc}\left(\frac{I_{\rm th}-I_0}{\sqrt{2}\sigma_0}\right).\right]. \quad (3)$$

When the optimum reference threshold current $I_{\rm th} = (\sigma_0 I_1 + \sigma_1 I_0)/(\sigma_0+\sigma_1)$ is selected, the channel minimum BER can be given by

$$P_{\rm e} = \frac{1}{2}{\rm erfc}\left[\frac{Q}{\sqrt{2}}\right] \quad (4)$$

where $Q = (I_1 - I_0)/(\sigma_0+\sigma_1)$ is the Q factor at the decision circuit.

B. Channel BER With Sinusoidal Interference

When an additional current interference is added at the input of the receiver, it is translated into the voltage disturbance signal at the decision circuit. This disturbance signal could be either added to the data channel or to the threshold reference channel. In both cases, it introduces extra noise to the comparator and increases the channel BER. With an additional sinusoidal interference signal having an amplitude of A and a random phase, the upper bound of channel BER can be approximated by [5]

$$P_{\rm e} = \frac{1}{2}\left[{\rm erfc}\left(\frac{Q-\rho}{\sqrt{2}}\right)\right] \quad (5)$$

where $\rho = A/\sigma$, A is the ratio of the interference amplitude, and σrms noise . Equation (5) is based on the interference signal that has a random phase with respect to the data stream. In practice, a sine wave whose frequency is substantially different from, and is not harmonically related to, the data rate can serve this purpose. Equation (5) indicates that the amplitude of the sinusoidal interference signal directly impacts the BER value, which implies that channel BER can be changed by controlling the amplitude of the interference signal. The BER in the absence of artificially introduced noise can be obtained from (5) by setting the interference signal to zero.

III. BER Extrapolation Technique

One of the most commonly used methods of BER measurement involves the transmission of a pseudorandom binary sequence (PRBS) through the data link with the error rate

computed by comparing received bits with a replica of the transmitted bit pattern. To get a close estimate of the system performance, a large number of bits needs to be transmitted to allow a sufficient number of errors to occur ($\sim$ 100 s). Therefore, the measurement time becomes unacceptably long for systems with very low BER, making the conventional method of testing impractical for such links.

To reduce the BER measurement time, it is possible to artificially degrade the channel in a controlled manner so that the error rate is raised substantially higher than the actual BER, to the range of 10^{-4} to 10^{-10}. These resultant error rate measurements are then extrapolated to determine the true BER of the data link.

As expressed by (5), the channel BER in the presence of a sinusoidal interference signal is given by the complementary error function within an order magnitude, in range of 10^{-4} to 10^{-30}. For that range, the complementary error function can be approximated to within 2% by [5]

$$\operatorname{erfc}\left(\frac{x}{\sqrt{2}}\right) = \exp\left[-c_1 x^2 - c_2 x - c_3\right] \tag{6}$$

where the coefficients are $c_1 = 0.4926$, $c_2 = 0.2498$, and $c_3 = 0.7912$. Therefore, an approximate expression for channel BER is given by

$$P_{\mathrm{e}} \approx \frac{1}{2}\exp\left[-c_1 (Q-\rho)^2 - c_2 (Q-\rho) - c_3\right]. \tag{7}$$

Solving for $(Q-\rho)$, we obtain [5], [6]

$$\Psi(P_{\mathrm{e}}) = Q - \rho = \frac{-c_2 + \sqrt{c_2^2 - 4c_1\left(c_3 + \ln(2P_{\mathrm{e}})\right)}}{2c_1}. \tag{8}$$

Since $\rho = A/\sigma$, we have an expression for $\Psi(P_{\mathrm{e}})$ that varies linearly with the amplitude of the sinusoidal interference signal A. Thus, using this expression, we can fit a straight line to the BER measurements with respect to A, and the zero-intercept obtained by extrapolation gives the estimate of Q. Then, the actual BER of the data link can be calculated as

$$P_{\mathrm{e}} \approx \frac{1}{2}\exp\left[-c_1 Q^2 - c_2 Q - c_3\right]. \tag{9}$$

Fig. 1 shows an example of implementing the extrapolation technique where a Q of 9.6 is obtained, yielding a BER of $3.9{*}10^{-22}$.

The following steps detail the procedures of the extrapolation technique.

1. Select an interference signal with a proper frequency and apply it to the receiver.
2. Adjust the amplitude of the interference signal until a BER of approximately 10^{-4} is observed.
3. Incrementally decrease the amplitude of the interference signal and measure the BER at each increment.

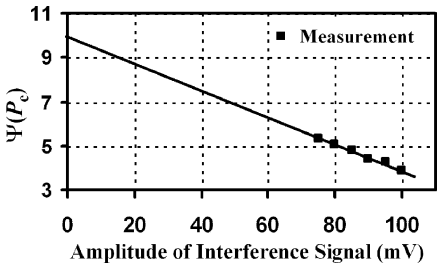

Fig. 1. Plot $\psi(P_{\mathrm{e}})$ versus the amplitude of sinusoidal interference signal shows the extrapolation techniques for an accelerated BER measurement. A straight line is fit to the measurements and extrapolated to the ordinate for the value of Q.

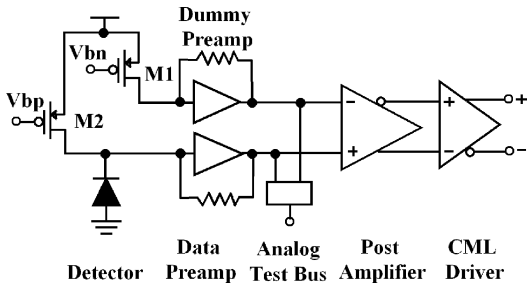

Fig. 2. Building blocks of the optical receiver design. It consists of two preamplifiers, a three-stage fully differential postamplifier, and a CML driver.

4. Calculate and plot the value of $\Psi(P_{\mathrm{e}})$ versus the amplitude of the interference signal.
5. Fit a straight line to the plot, extrapolate the y-intercept, and get the intersect value with $\Psi(P_{\mathrm{e}})$ axis for Q.
6. Substitute the value of Q into **(9)** to get the BER value for the link in the absence of artificially introduced noise.

IV. Hardware Implementation

A 1×4 optical transceiver chip was designed to verify the integrated accelerated BER measurement technique. It is integrated with additional interface circuits that allow an external interference signal to be added into the receiver to provide more flexibility during the testing. A BERT was implemented in an FPGA, and a free-space optical interconnect system was built to demonstrate the proposed technique.

A. CMOS Integrated Circuit Design

1) Optical Receiver Design: The goal of the receiver design is to facilitate the verification of BER extrapolation techniques by providing various flexible interfaces for testing. Fig. 2 shows the main blocks of the receiver design. It consists of two preamplifiers, a three-stage postamplifier, and a current mode logic (CML) driver. One data preamplifier is directly connected to a photodetector and converts the current input to a voltage signal for the next stage. One dummy preamplifier is designed to generate a dc threshold voltage for the decision circuit for data comparison. The purpose of using two preamplifiers is to

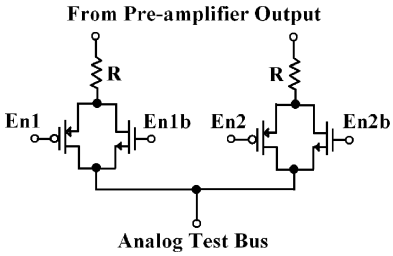

Fig. 3. Schematic of an analog test bus in receiver design that allows selectively probing the outputs of preamplifier by enabling the transmission gate.

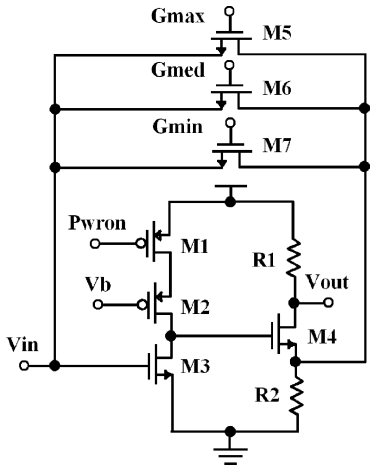

Fig. 4. Schematic of a transimpedance amplifier design shows three digital gain settings suitable for a wide dynamic range of current input.

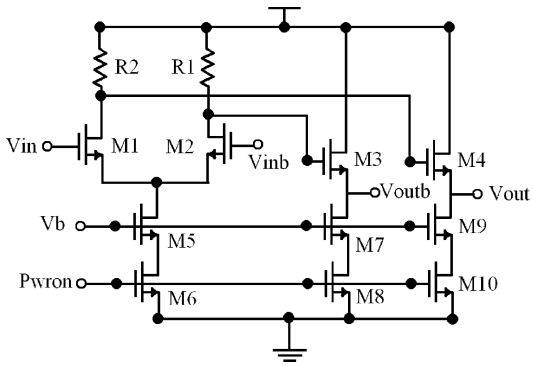

Fig. 5. Schematic of a fully differential postamplifier design.

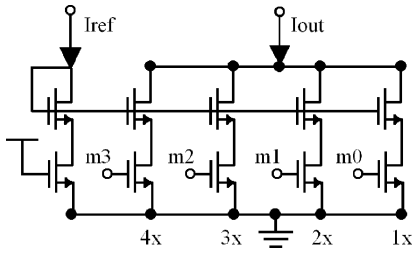

Fig. 6. Schematic of a current-mode DAC.

achieve a better matching between the data and the threshold voltage channel. The decision circuits and postamplifiers consist of three stages of fully differential amplifiers for data recovery and waveform shaping. Finally, the CML driver is used to send the data off-chip electrically.

The most unique part of our design are the two dummy p-type metal–oxide–semiconductor (PMOS) transistors, identified as M1 and M2 in Fig. 2, with their drains and sources connected between the power supply and the input of two preamplifiers. A dc voltage Vbn, applied to the gate of M1, induces a constant current flowing into the preamp, which sets a dc threshold voltage for the decision circuit. More important, an ac interference current signal can be introduced into the data or dummy channels by imposing an ac signal at Vbn or Vbp with a proper bias voltage. Since the ac current induced is proportional to the ac voltage signal at the gate, the dummy PMOS transistors provide a method of introducing an amplitude-controllable current interference to the receiver. In addition, this design feature also allows testing the receiver ac performance by injecting ac current into the preamplifier without the need of integration with optoelectronic (OE) devices.

Another feature of our design is an analog test unit connected to the output of the two preamplifiers. As shown in Fig. 3, this analog test unit uses a transmission gate together with a 50-kΩ resistor in series, which allows monitoring the analog output of the preamplifier by enabling the transmission gates digitally. Using a large serial resistor minimizes the impact on channel performance. The voltage of the analog output is the average value of transmitted transition-rich data. Therefore, it provides a reference voltage at which the optimum threshold voltage should be set in the dummy channel for the decision circuits. It also provides a gauge of the optical power received by the detector, which facilitates optical alignment during system integration.

Figs. 4 and 5 show the schematics of the transimpedance amplifier (TIA) section of the preamplifier and one stage of the postamplifier. Three digital inputs ($G\min$, $G\mathrm{med}$, and $G\max$) are the digital gain control inputs, which, when enabled, give 1-, 2.5-, and 10-kΩ transimpedance gain, respectively. Both amplifiers have a power-control transistor that can turn off the amplifiers using digital control signals to reduce power consumption when the link is idle. The CML driver circuits have 100-Ω differential output impedance and can deliver a 400-mV differential peak–peak output.

2) Optical Transmitter Design: Since the light output of a VCSEL is linearly proportional to its driving current in the normal operating range, the goal of the driver design is to provide accurate tunable modulation and bias current for the VCSELs. Two four-bit current-mode digital-to-analog converters (DACs) are used to provide digital control over the modulation and bias current supplied to the VCSEL. The control settings are loaded and stored in register-based digital storage cells. Therefore, this current-mode DAC-based transmitter design allows great flexibility in adjusting the power level during experiments to compensate for a very wide range of optical loss due to a nonideal operating environment.

Fig. 6 shows the schematic of a current-mode DAC with 4-b digital control inputs m0–m3. It is based on a current mirror structure, and the transistors in each mirrored branch are sized proportionally so that each bit has different significance of current control. The reference current input I_{ref} is the step size for

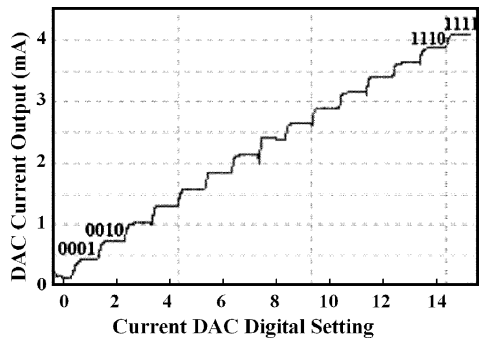

Fig. 7. Simulation of transmitter current stepping while sweeping the digital power setting shows the accurate linear current output control.

current tuning and can be adjusted externally by the user to suit the requirements of different systems.

Fig. 7 illustrates the current output of the bias DAC in the transmitter while sweeping the digital settings from "0000" to "1111" with a step size of $I_{\rm ref}$. Careful circuit design ensures the linearity of current stepping, which provides precise control over the driving current for VCSELs.

3) Design Overhead for Integrated BER Measurement: Due to the very limited chip area available in our fabrication, the BERT and extrapolation functions are not directly integrated on our optical transceiver chip. In practice, it is possible to incorporate them into an optical transceiver chip. A BERT usually consists of a PRBS generator and a verifier. For a 15-b sequence, it could take approximately 300×400 μm in a 0.5-μm process and consume 140 mW at 1.5 Gb/s based on our estimation. in addition, parallel electrical transceivers that include on-chip BERT are commercially available [16]. The extrapolation circuitry mainly performs standard mathematical functions and may consist of standard arithmetic digital modules. Alternatively, it can be efficiently implemented in a system that already includes a microcontroller, as do some commercial optical modules [17].

The on-chip noise generator and the additional circuits for introducing interference do not significantly impact the overall noise, speed, and power consumption of the receiver. The dummy transistors M1 and M2 add a mere 6.7 fA/$\sqrt{\rm Hz}$ noise to the preamplifier, which has an input referred current noise of 4.1 pA/$\sqrt{\rm Hz}$ and a sensitivity of 40 μA, when the gain setting $G{\rm med}$ is enabled. The maximum parasitic capacitance of M1 and M2 are each less than 10 fF and can be largely ignored considering the $\sim$ 400-fF capacitance from the photodiode and packaging, resulting in very little impact on the receiver bandwidth. The interference signal can be generated using an on-chip oscillator, and its amplitude can be modulated using current-mode DACs. The operating power consumption of this circuit is around 0.6 mW. This is due to the fact that only a very small amount of current is needed for interference signals for testing purposes, and it can be completely turned off during normal data transmission. Each DAC consumes an area of 60×18 μm in a 0.5-μm process.

B. CMOS Technology and Chip Layout

Our chip was designed and fabricated in the Peregrine Semiconductor 0.5-μm ultrathin silicon-on-sapphire (UTSi/SOS) process. UTSi is a silicon-on-insulator (SOI) technology where devices are made in a very thin silicon layer (100 nm) on top of an insulating sapphire substrate. As any other SOI technologies, the elimination of silicon bulk substrate brings various advantages for analog and mixed-circuit design, including low power consumption, reduced parasitic capacitance, and minimum crosstalk. In addition, the substrate sapphire is transparent at a wavelength of 850 nm, which is ideal for flip-chip integration with top-emitting OE devices. Sapphire is also a very good thermal conductor, and its thermal expansion coefficient is more closely matched with the gallium arsenide (GaAs) of the OE devices than bulk silicon.

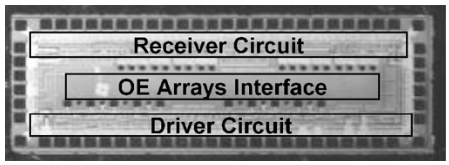

Fig. 8. Micrograph of a 1×4 optical transceiver CMOS integrated circuit (IC).

In an area of 4.4 $\times$ 1.5 mm, four single-ended optical transceivers are implemented with 64 perimeter pads and 16 pairs of flip-chip bonding pads in the center for OE array integration. A micrograph of the chip is shown in Fig. 8. The driver and receiver circuits are 650×75 μm and 740×77 μm, respectively.

The chip was manually laid out using the custom layout tool from Cadence, and transistor-level simulation was performed using Spectre. Special care was taken at the layout level to ensure signal integrity. Power and ground rails were separated for analog and digital circuits, and an interleaving scheme and a dual-gate structure were used for better matched dual preamplifiers and differential circuits. In addition, dummy gates, decoupling capacitors, and electrostatic discharge (ESD) circuitry were included [18].

C. System Integration

1) Integration of CMOS Chip With OE Device: The OE devices used are an Emcore high-performance 1×4 VCSEL and a 1×4 GaAs p-i-n photodiode arrays on a 250-μm pitch. The VCSEL has a wavelength of 850 nm, a typical slope efficiency of 0.45 mW/mA, and a differential resistance of 50 Ω. The p-i-n photodiodes have a typical responsivity of 0.5 A/W and a capacitance of 0.4 pF. They are both rated for 3.125-Gb/s applications.

Since flip-chip bonding offers low parasitic capacitance and high integration density, it is chosen for the integration of the CMOS chip with the OE devices. Since both VCSEL and photodetector arrays are top-emitting devices, the laser beams emit through the sapphire substrate of the CMOS chip during their operation.

2) Chip-on-Board (COB) Packaging: A 2 $\times$ 1.5-in printed circuit carrier board was designed and fabricated. The hybrid CMOS chip with the OE arrays attached is placed in the center of the carrier board and wire-bonded to it. Directly underneath the hybrid CMOS chip, a 4.5×1.2-mm^2 opening has been made on the carrier board for optical access. Fig. 9 shows the front view of the CMOS hybrid chip attached to the carrier board with wire bonds.

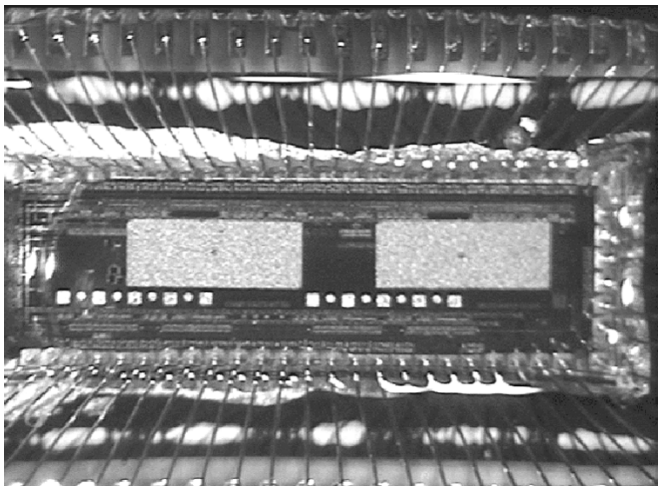

Fig. 9. Micrograph of the chip-on-board packaging. Two photodetector arrays are attached to the transceiver chip by the flip-chip process, and the hybridized CMOS chip is wire-bonded to the carrier board.

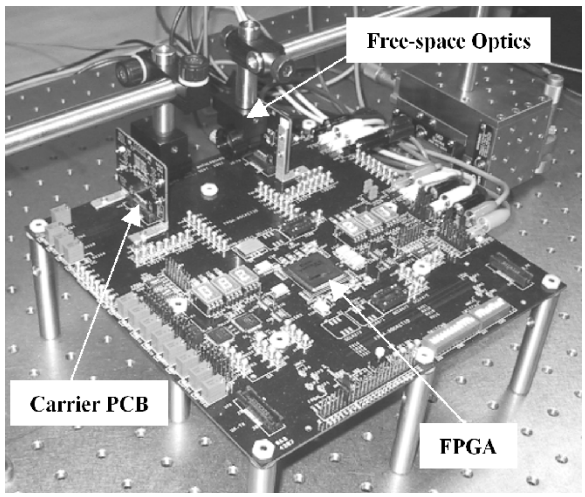

Fig. 10. Overview of the demonstration system. It integrates two carrier boards, a Virtex II Pro FPGA, and the free-space optics mounted on micro-positioning stages.

3) Motherboard: A ten-layer, 8.5 $\times$ 8.5-in FR4 motherboard was designed and fabricated for final system integration. Two carrier boards were connected perpendicularly to the motherboard simultaneously by using Mictor impedance-controlled connectors. Right-angle metal clamps were used to stabilize the attachment. The demonstration system is shown in Fig. 10.

A high-performance FPGA (XC2VP7) from the Xilinx Virtex-II Pro family was used as a central control unit. Connections were made between the FPGA and each carrier board. Various mechanical structures were incorporated to enhance system stability and facilitate system testing. The whole setup was assembled on top of an optical breadboard, which provided good vibration isolation.

The FPGA selected integrates eight full-duplex multigigabit serial transceiver cores (RocketIO) capable of baud rates up to 3.125 Gb/s. In addition to the embedded serializer and deserializer (SERDES), it also includes monolithic clock synthesis and clock data recovery (CDR) circuits with optional 8B/10B encoder and decoder, supporting a number of high-speed standards, including fiber channel, gigabit Ethernet, and Infiniband. The CML I/Os are used for high-speed data transmissions, allowing selectable transmission (TX) and receiver (RX) impedance termination, a configurable pre-emphasis level, and a programmable output differential voltage range. All these features provide great flexibility in system testing.

D. Free-Space Optical Interconnection

A free-space optical interconnection system was used to establish communication links between two chips. Two seven-element Universe Kogaku f-1.2 lenses are used to link a pair of carrier boards, separated by 89 mm. A charge-coupled device (CCD) camera allowed direct observation of both the VCSEL and detector arrays to facilitate in the alignment process. The voltage drop of the receiver preamplifier output through the analog test bus is monitored during the active alignment process when the VCSELs are turned on. Due to the large disparity between the resolution of the incident spots (full-width-at-half-maximum $\approx 50\ \mu$m), and the separation of the detectors (250 μm), there was no detectible optical crosstalk between adjacent channels. In addition, with only four channels and very little scattering, there was not a significant level of ambient light.

V. Experimental Results

A. Test Setup Overview

The purpose of this test was to determine the BER of an optical link using our accelerated BER extrapolation technique in a practical serial data transmission system, where SERDES and CDR circuits are normally used. An FPGA with integrated serial transceivers was used to fulfill such test needs. All experiments are carried out based on the custom-built test-bed described previously, and the system block diagram is shown in Fig. 11.

Four optical links were established between the transmitter and receiver chips via a free-space optical system. The FPGA sources and sinks data through the RocketIO serial transceivers and also configures the optical transceiver chips through low-speed lines. The BERT was implemented on the FPGA, and a PRBS pattern of $2^{20} - 1$ was selected for this testing. A custom interface was developed on the FPGA to allow the user application code to communicate with the RocketIO serial transceivers, and the data were exchanged in parallel between the two. In order to reflect the actual performance of the data link, the 8B/10B and CRC coding and decoding options of the RocketIO were bypassed and disabled during the testing process.

Initial tests were carried out to verify the functioning of the BERT logic and the integrity of the electrical data links between the RocketIO transceivers. Artificial errors were introduced through hardware description language (HDL) coding to the BERT to verify its error detection functionality. Test results showed that the BERT was able to detect bit errors and display the total number of those errors correctly on the light-emitting diodes (LEDs) on the motherboard. The final logic functions were tested by running the RocketIO transceivers in the electrical loop-back mode for several hours, and no errors were detected. To test the stability of the optical system, the demonstration

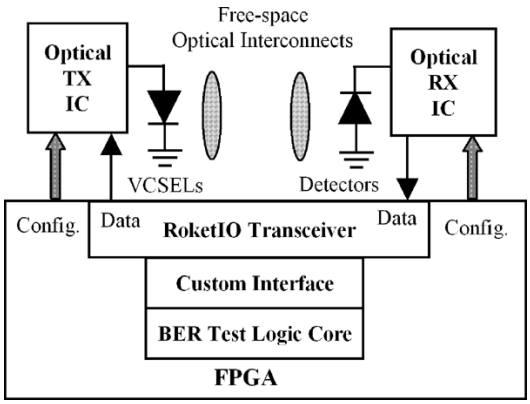

Fig. 11. Block diagram of the test setup overview. FPGA generates and receives pseudorandom sequence to perform BER test. Embedded RocketIO in FPGA communicates with the optical transceivers at a data rate of 1.5 Gb/s.

system was run continuously for eight hours, and likewise no errors were detected.

To test how fast our optical transceiver could operate, a pattern generator was used to send a PRBS to the transmitter, and the output of the receiver was monitored by an oscilloscope. Fig. 12 shows the eye diagram of the receiver output at 2 Gb/s. Although the bandwidth of our transceiver design is > 2 Gb/s, all experiments were conducted at 1.5 Gb/s, which was limited by the clock oscillator available at the time of experiment.

An arbitrary waveform generator (AWG), AWG610 from Tektronix, was used to generate an ac signal as the artificial interference signal to degrade the channel performance. The AWG used is capable of outputting differential ac signals with peak–peak values of 20 mV to 2 V, at 1-mV resolution, up to several hundred megahertz. Although a wide range of different waveforms is available, the square waveform and sinusoidal waveform are selected as the interference signals. Fig. 13 shows the details of signal connections. In [19], a sinusoidal interference signal frequency between 100 MHz and 2 GHz is suggested for stressed receiver testing in 10-Gb/s Ethernet applications. Here, both 70- and 110-MHz frequencies were selected for the interference signal in a 1.5-Gb/s link, which was well within the pass band of the bias tee and the optical receiver and was completely independent of the data received.

A bias tee was used to provide a dc-bias voltage for the dummy PMOS (M1 or M2). The bias voltage was carefully chosen to ensure M1 or M2 were well within the saturation region so that any given small ac voltage interference resulted in an ac current to the pre-mplifier that varied linearly with respect to its voltage amplitude. Therefore, it is accurate to use the voltage amplitude of the ac interference for extrapolation rather than the amplitude of the induced current. The following sections detail specific experiments that were conducted.

B. Interference Introduced Into the Dummy Channel

In this setup, the optimum threshold voltage was intentionally corrupted to degrade channel performance by introducing an ac interference signal to the dummy channel. It was done by connecting the output of the AWG to M1 with a dc-bias voltage applied from the bias tee, as shown in Fig. 13. Thus, the dc-bias voltage not only ensured biasing M1 in the saturation region, it

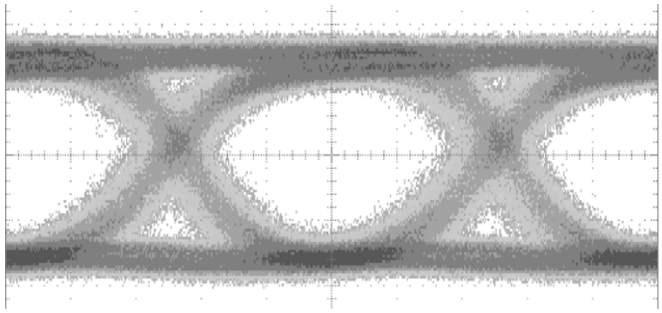

Fig. 12. Eye diagram of the receiver output at 2 Gb/s during the link test.

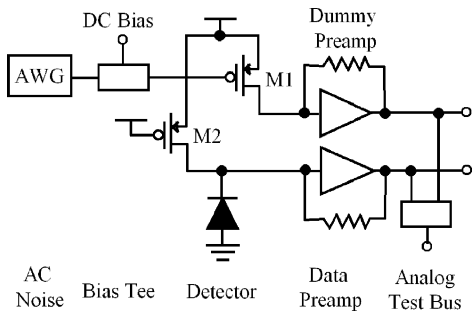

Fig. 13. Block diagram of the test setup shows that an interference signal from an AWG is connected to the PMOS M1 together with a dc-bias voltage through a bias tee.

also generated an optimum threshold voltage for decision circuits. The PMOS M2 in the data channel was turned off by applying a voltage of 3.3 V at the gate so that the receiver is only amplifying the current induced in the photodetector.

Both a sine wave and a square wave were chosen as the interference signals, and the amplitude ranging from 120 to 60 mV was selected for each measurement with dc-bias voltage of 1.0 V. VCSEL modulation and bias currents were set at 1.5 and 1.2 mA, respectively, which gave an average output optical power of 400 μW with an extinction ratio of 6.2 dB. This optical power was kept fixed throughout measurement, and the received power was around 100 μW, which could be tuned by placing an optical filter in the optical path. At 1.5 Gb/s, our transmitter and receiver consumed an average power of 22 and 24 mW, respectively. Every measurement was taken after running long enough to allow more than a hundred errors to occur, yielding a high-confidence BER estimate of the link. The total number of errors were displayed in numeric displays on the motherboard after each measurement, and the value of $\Psi(P_{\rm e})$ was calculated according to (8).

Fig. 14 plots the value of $\Psi(P_{\rm e})$ versus the amplitude of the ac interference signal for the two cases where a sine wave and a square wave are used. It can be seen that steeper slope occurs for the square-wave interference case, which can be explained by the tendency of the square-wave interference to generate more errors than the sinusoidal interference for the same amplitude. This is because the square-wave oscillates between two constant noise-degrading impact levels, while the sinusoidal wave transitions smoothly and only reaches this maximum impact level twice per cycle. The curves are extrapolated to their zero interference points, giving a Q value of 6.75 for both. This Q is substituted into (9), resulting in an estimated BER of $1.3{*}10^{-11}$.

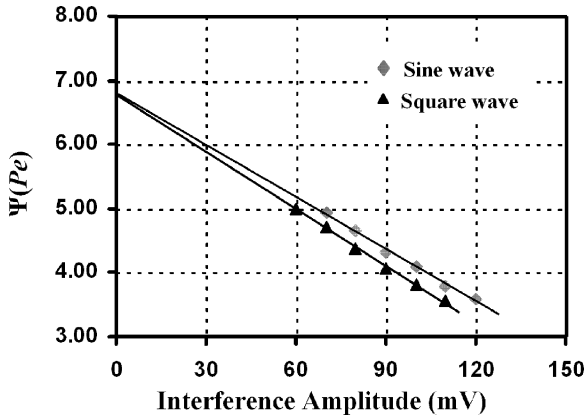

Fig. 14. Plot of $\Psi(P_{\rm e})$ versus the amplitude of the interference signal, which is presented in receiver dummy channel. The measurements of both square wave and sine wave are extrapolated to the $\Psi(P_{\rm e})$ axis, resulting in the same value of Q at 6.75.

This procedure was repeated using an interference signal of 110 MHz to explore other interference frequencies that can be used for extrapolation, and it resulted in the same extrapolated value for link BER.

To verify the actual BER of the link, the same setup was run continuously for 10 h, without the artificial interference. A total of 240 errors were detected over that period, which yields a BER of $1.4{*}10^{-11}$. This shows the close match between the estimated value using the accelerated measurement technique and the actual link BER.

To visually show how the artificial interference degrades the link performance, a number of eye diagrams with different interference signal amplitudes are shown in Fig. 15. It can be seen that the eye opening becomes bigger and, consequently, the BER improves as the interference signal amplitude is decreased from (a) to (d).

C. Interference Signal Introduced Into the Data Channel

In this test, an ac interference signal was introduced to the data channel to degrade channel performance while keeping the optimum threshold voltage generated by the dummy channel fixed. The output of the AWG was connected to M2 with a 1.5-V bias voltage, applied using a bias tee. Both a sine wave and a square wave were selected for the ac interference signals. Fig. 16 plots the value of $\Psi(P_{\rm e})$ versus the amplitude of the ac interference signal. It can be seen that the same value for Q of 6.75 is extrapolated for both interferences. Again, the estimated BER of $1.3{*}10^{-11}$ agrees with the measured actual link BER.

D. BER Measurements With Varying Optical Power

Multiple BER measurements using conventional and accelerated methods over a range of optical power levels were carried out by attenuating the optical power with different optical filters between the two lenses. Fig. 17 shows the BER value versus normalized optical power for the data link. Points marked as rectangles are the measured BER using the conventional method. Points marked as triangles are the extrapolated BER with a 110-MHz sinusoidal interference injected into the dummy channel. The horizontal axis shows the additional power attenuation in decibels introduced by the optical filters. The solid line is drawn for a link where Gaussian noise dominates, according to (4). The plots show the close match for the measurements between two methods as well as the close match between measurements and theoretically predicted values,

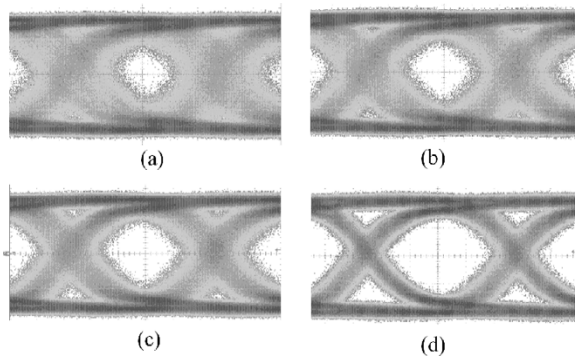

Fig. 15. Eye diagrams of the optical receiver at 1.5 Gb/s with interference signal of different amplitude A present in the dummy channel. (a) A = 100 mV, BER = $6.5{*}10^{-5}$. (b) A = 80 mV, BER = $5.8{*}10^{-6}$. (c) A = 60 mV, BER = $3.8{*}10^{-7}$. (d) A = 0 mV, BER = $1.4{*}10^{-11}$.

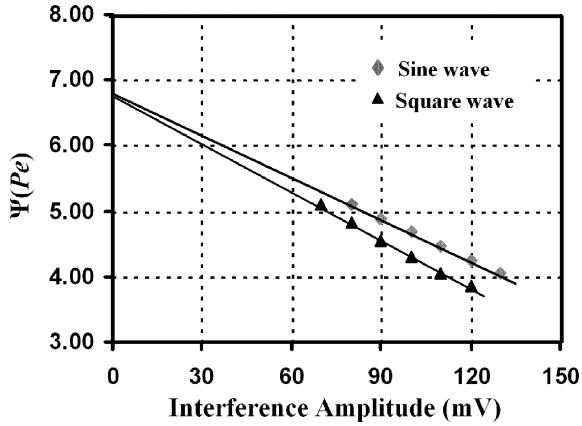

Fig. 16. Plot of $\psi(P_{\rm e})$ versus the amplitude of the interference signal presented in the receiver data channel. The measurements of both square wave and sine wave are extrapolated to the $\psi(P_{\rm e})$ axis, resulting in the same value of Q at 6.75.

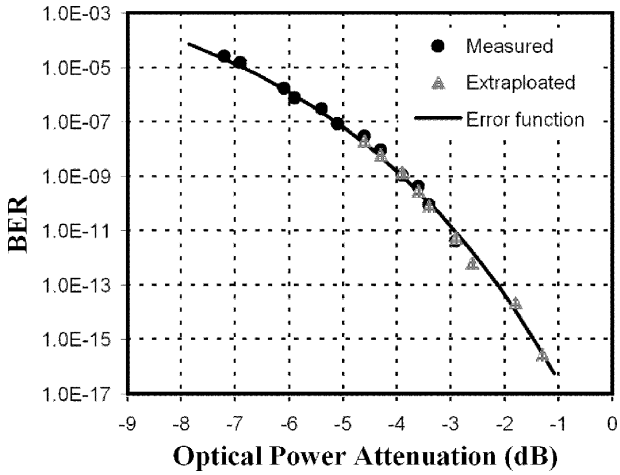

Fig. 17. Plot of BER versus the optical power attenuation for a 1.5-Gb/s optical link. Close matching is observed among the measured BER (dots), extrapolated BER (triangles), and the complementary error function plot.

which further proves the validity of the proposed accelerated BER measurement technique.

E. Discussion

The experimental results show that accelerated BER measurement can be performed using our optical transceiver design to determine the actual link BER with high confidence. The same BER value can be extrapolated by using either a square-wave or a sinusoidal-wave interference signal. Introducing artificial noise signals to either data channel or threshold voltage channel has the same effect on degrading channel performance for a dc-coupled optical receiver, and thus, both approaches can be used for accelerated BER measurement. This technique can also be extended to an ac-coupled receiver, where an interference signal is introduced into the data channel. The results also show that different frequencies can be used for interference signals, provided that the signal is data independent and not harmonically related to the data rate.

Our experimental setup used a free-space optical interconnection system, which experienced no measurable levels of optical crosstalk or ambient light due to scattering. In this particular system, Gaussian noise approximation is applicable and emphasized by the close correlation between the measured data and the curve in Fig. 17. In other systems that suffer from non-Gaussian noise sources, such as crosstalk, high aggregate levels of scattered light, or modal noise in fiber links, extending these techniques may require additional theoretical analysis using non-Gaussian noise models and experimentation. However, the methodology described here can serve as a starting point to accelerate the functionality verification of such links.

VI. Conclusion

This paper presents an optical transceiver architecture with accelerated BER measurement capability. A theoretical framework is presented to show the application and validity of our architecture. A 0.5-μm CMOS, 2-Gb/s, four-channel, optical transceiver was designed, fabricated, and tested to serve as a vehicle for verifying the proposed architecture. Although some of the circuits were implemented in an FPGA to reduce design time and risk, design overhead analysis and existing electrical transceivers show the feasibility of incorporating BER testing on-chip. The experimental results show excellent agreement between extrapolated and actual measured BER values. A BER of $1.3{*}10^{-11}$ has been extrapolated in the accelerated BER testing for a 1.5-Gb/s link, while a 10-hBER measurement shows the actual link BER to be around $1.4{*}10^{-11}$. Multiple BER measurements over a range of optical power levels show the close match between the measured BER, the extrapolated BER, and the BER predicted using the complementary error function. To the authors' knowledge, this is the first report of accelerated BER measurement that did not use specialized test equipment and successfully correlated extrapolated and measured optical link BER. The results point to the feasibility of incorporating accelerated BER measurement as an integral part of optical transceiver circuits. This capability is critical to the adoption of optical links in applications where "in the field" testing of system components is a critical requirement.

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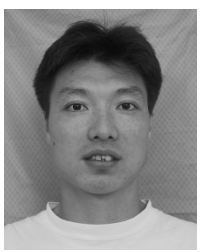

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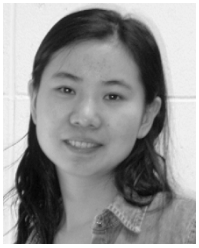

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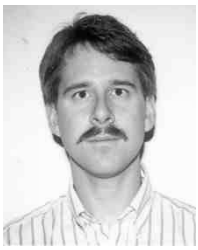

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